

VZ8A Block Diagram

PCB PTH Stackups

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : GND1
LAYER 8 : IN4
LAYER 9 : GND2
LAYER 10 : BOT

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : GND1
LAYER 8 : BOT

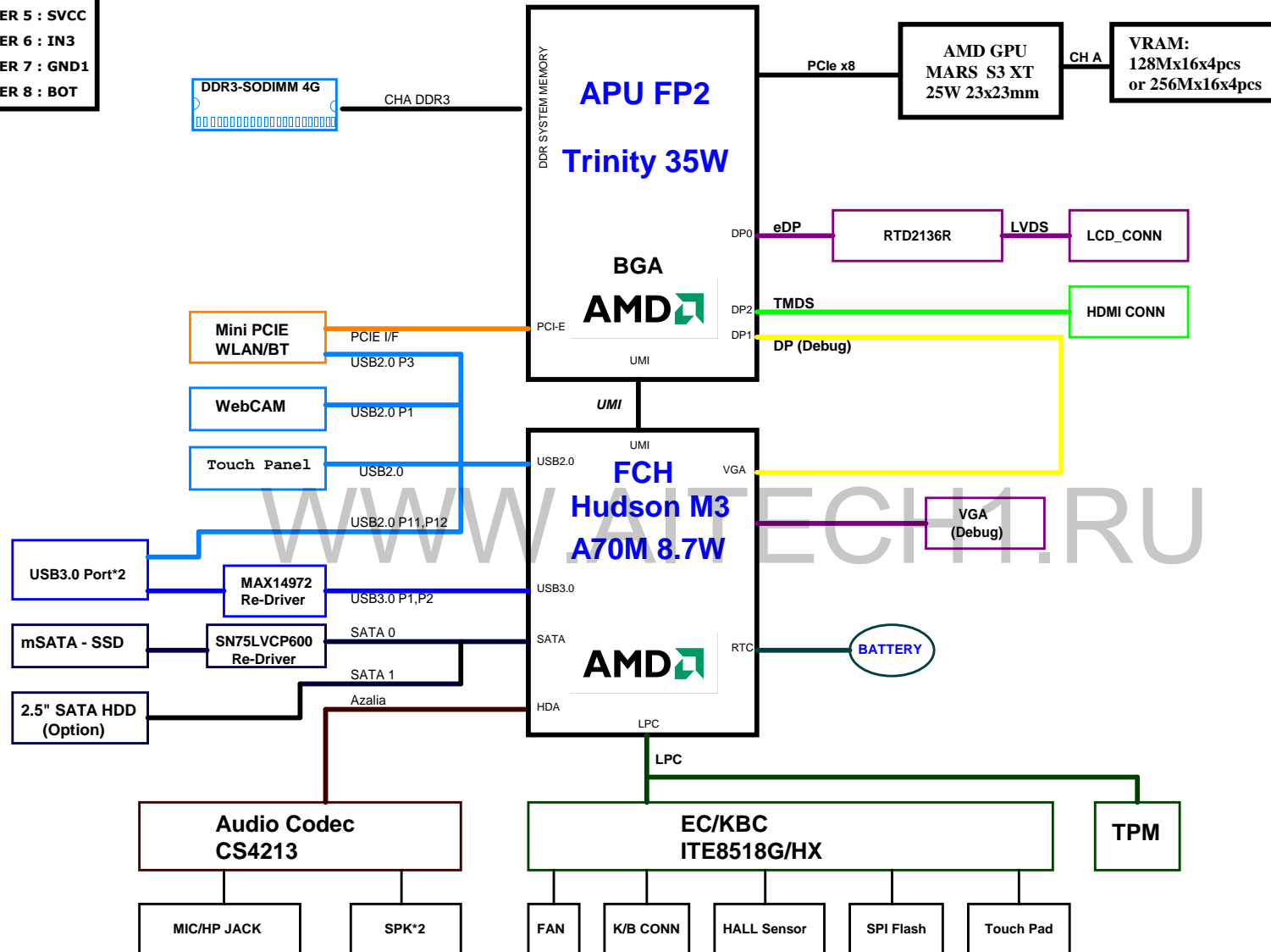


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Voltage Rails

Power	Voltage	S0	S3	S4/S5 (Wake support)	S5	G3	Ctl Signal	
3V_RTC	3V	ON	ON	ON	ON	ON		FCH, EC
VIN	19V	ON	ON	ON	ON	OFF	Adaptor in	
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in	
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in	Hall Sensor, EC, EC ROM
12V_S5	12V	ON	ON	ON	ON	OFF	Adaptor in	
3V_WLAN	3.3V	ON	ON	ON	OFF	OFF	WLAN_ON	WLAN
3V_S5_P	3.3V	ON	ON	ON	OFF	OFF	S5_ON1	FCH, BIOS ROM
5V_S5	5V	ON	ON	ON	OFF	OFF	S5_ON1	
3V_S5	3.3V	ON	ON	ON	OFF	OFF	S5_ON1	FCH, USB3 redriver, Codec
1V8_AUD	1.8V	ON	ON	ON	OFF	OFF	S5_ON1	Codec
1.1V_S5	1.1V	ON	ON	ON	OFF	OFF	S5_ON2	FCH
5V_S3	5V	ON	ON	OFF	OFF	OFF	S3_ON	LED, USB30, Touch module
1.5V_S3	1.5V	ON	ON	OFF	OFF	OFF	S3_ON	APU, So-Dimm
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON_1	HDMI, CRT, HDD, Codec, KB, FAN
3V_S0	3.3V	ON	OFF	OFF	OFF	OFF	S0_ON_1	SATA redriver, FCH, DIMM SPD, GPU
2.5V_S0	2.5V	ON	OFF	OFF	OFF	OFF	S0_ON_2	RTD2136R, TPM, SSD, panel, EC, TP board
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON_2	APU
DDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	S0_ON_2	APU debug, WLAN
1.2V_S0	1.2V	ON	OFF	OFF	OFF	OFF	S0_ON_2	So-Dimm
1.1V_S0	1.1V	ON	OFF	OFF	OFF	OFF	S0_ON_2	APU
NB_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON	FCH
CPU_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON	APU
8.5V	8.5V	ON	OFF	OFF	OFF	OFF	BL_LED_EN	APU
1.8V_VGA	1.8V	ON	OFF	OFF	OFF	OFF	DGFX_VR_PWRGD	LCD BL
1.5V_VGA	1.5V	ON	OFF	OFF	OFF	OFF	DGFX_VR_PWRGD	GPU(CORE, PLL)
PCIE_VDD	0.95V	ON	OFF	OFF	OFF	OFF	DGFX_VR_PWRGD	GPU(DDR)
VGA_CORE	By VID	ON	OFF	OFF	OFF	OFF	DGFX_VR_PWRGD	GPU(PCIE)
								GPU(CORE)

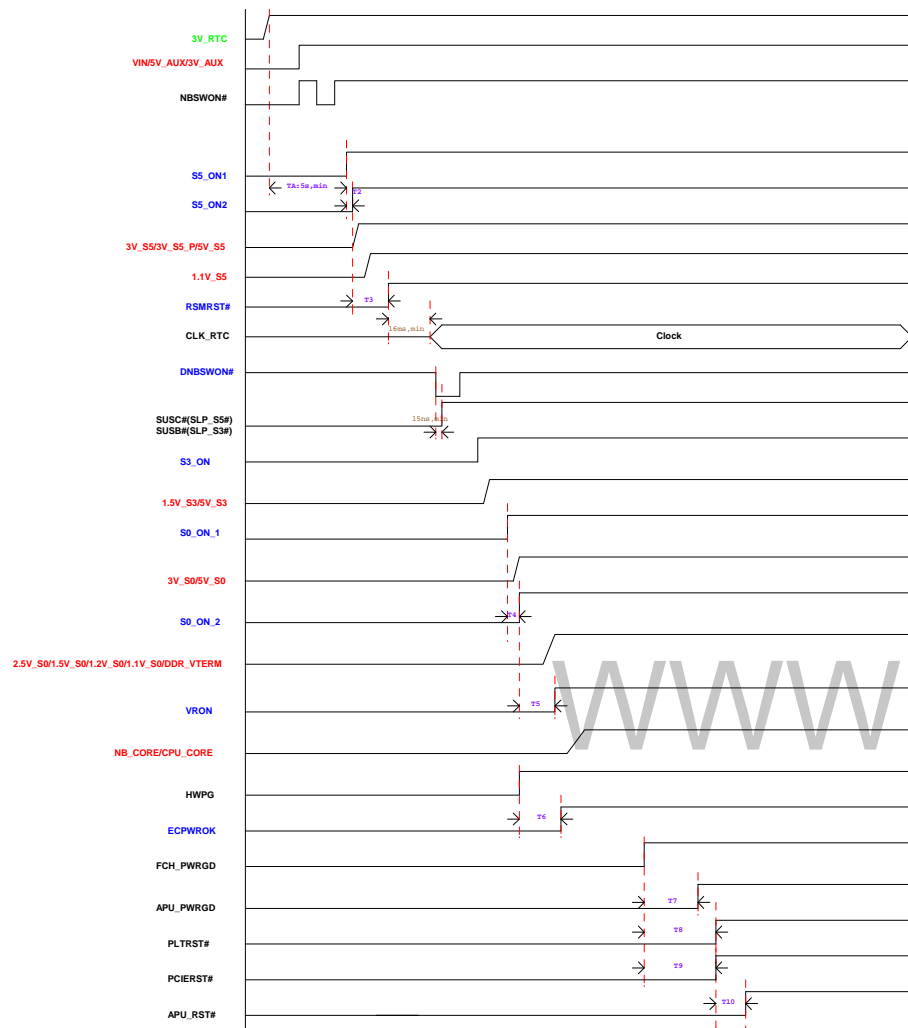


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PROJECT : VZ8A

Size	Document Number	Rev
	02 -- Power Stage& BOI-Function	1A
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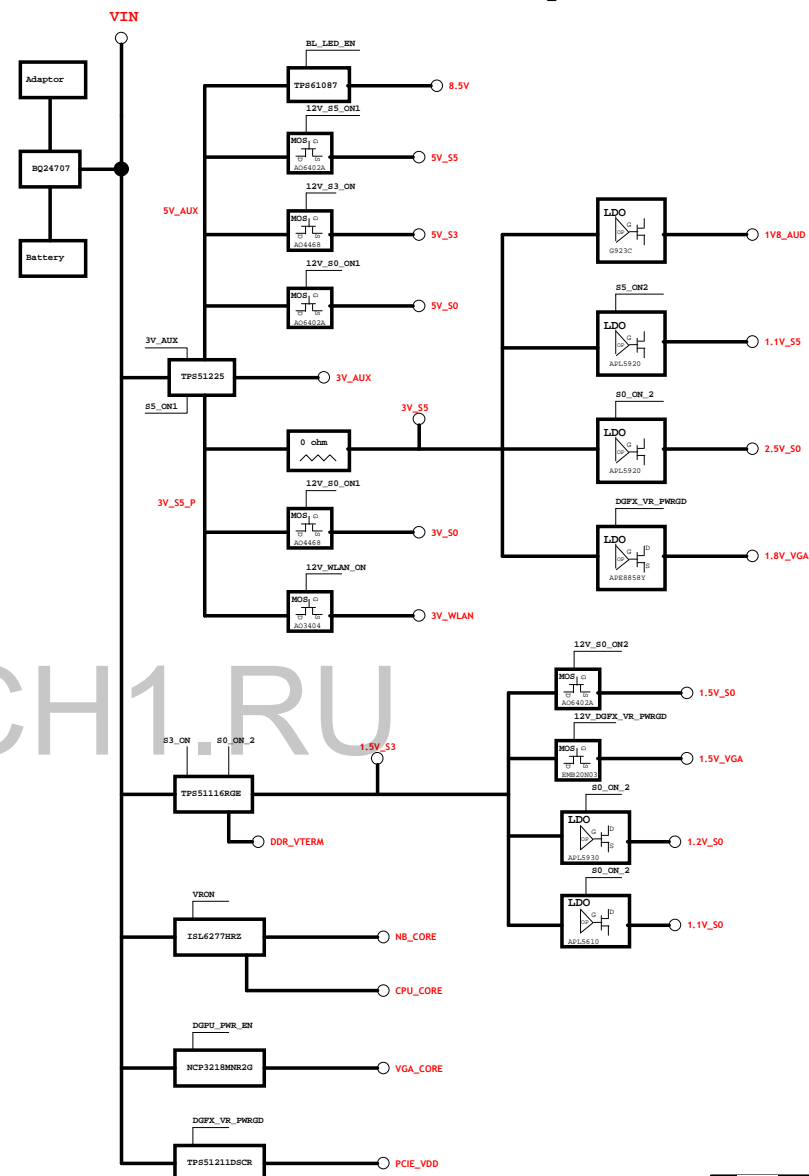
Power On Sequencing Timing Diagram



System Power Sequence

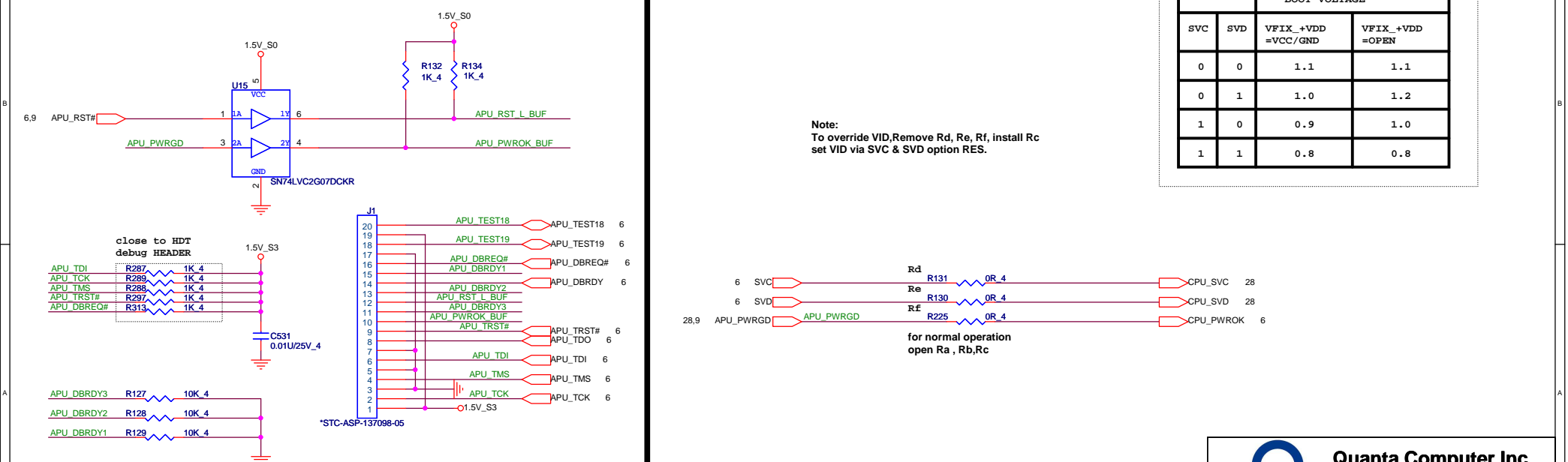
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Power Map



HDT+ Connector for Debug only **VID Override Circuit**

HDT+ Connector for Debug only **VID Override Circuit**



The schematic diagram illustrates the APU test board connections. Key components include the APU (J1), a buffer IC (U15, SN74LVC2G07DCKR), and various test points and resistors. The board is powered by 1.5V_S0 and 1.5V_S3. The APU test points are connected to the board headers. The buffer IC is used to drive the APU test points. The board is populated with resistors R127, R128, R129, R131, R130, R225, R267, R285, R286, R297, and R313. The board is labeled "STC-ASP-137098-05".

VDD1 VOLTAGE

SVC	SVD	VFIX_+VDD =VCC / GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Note:
To override VID, Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.

for normal operation
open Ra , Rb, Rc

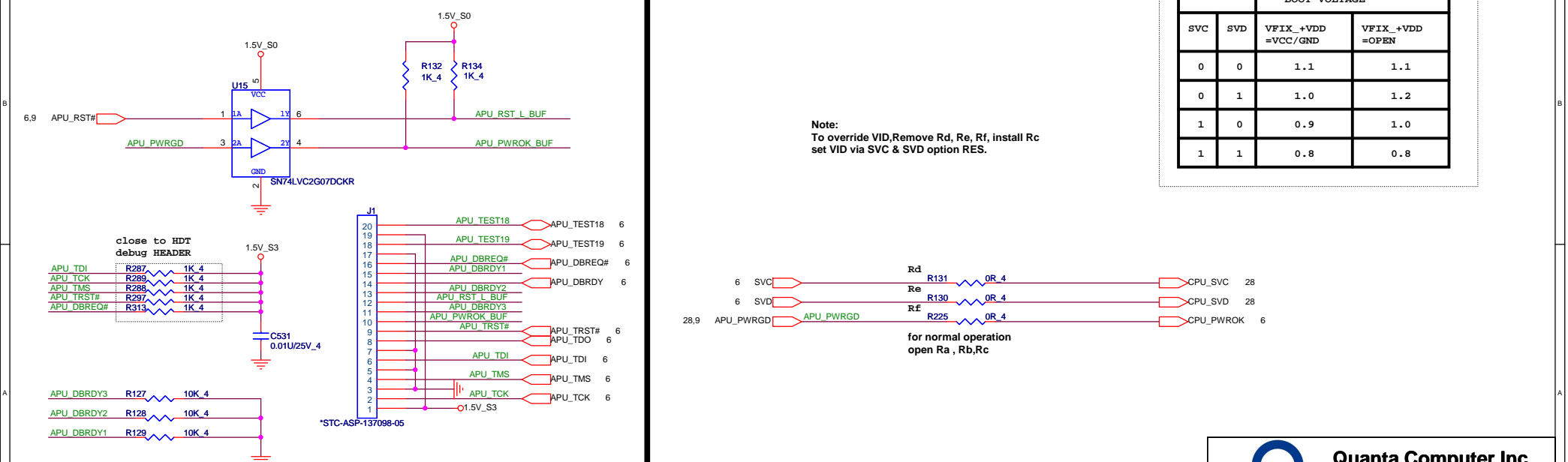
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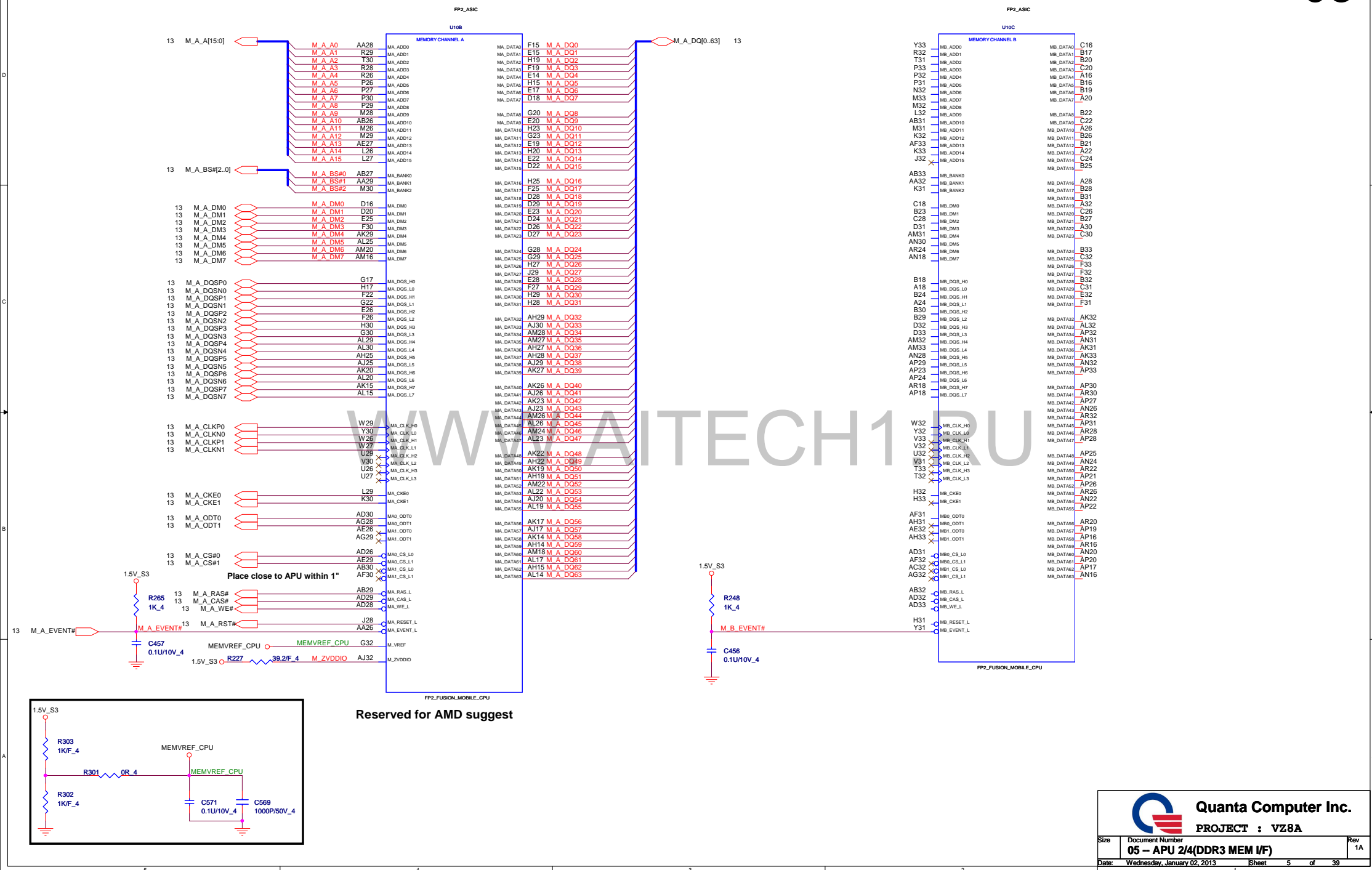
VDD1 VOLTAGE

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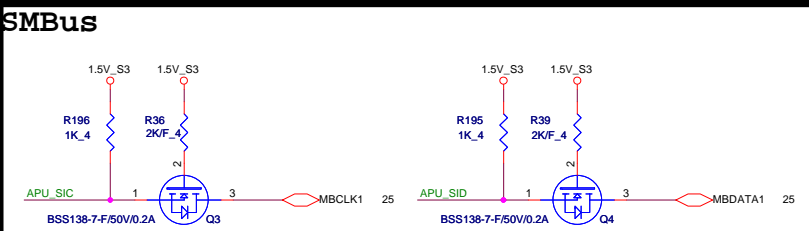
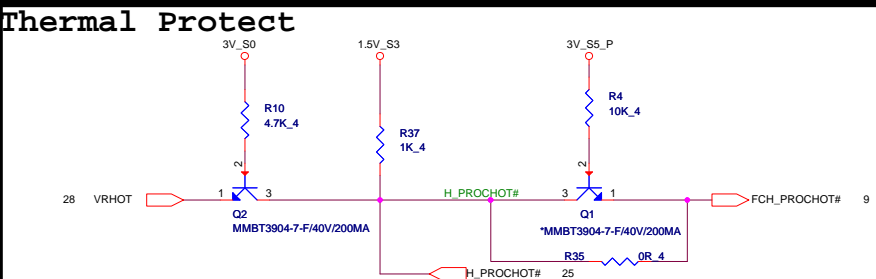
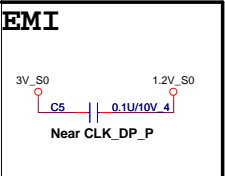
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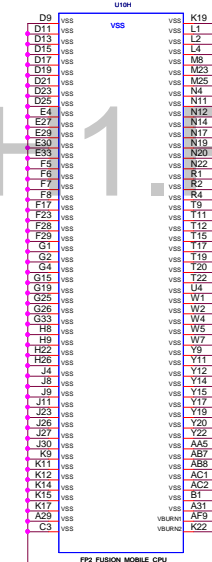
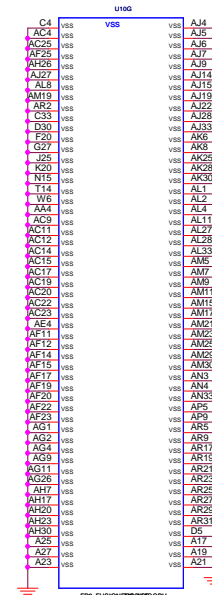
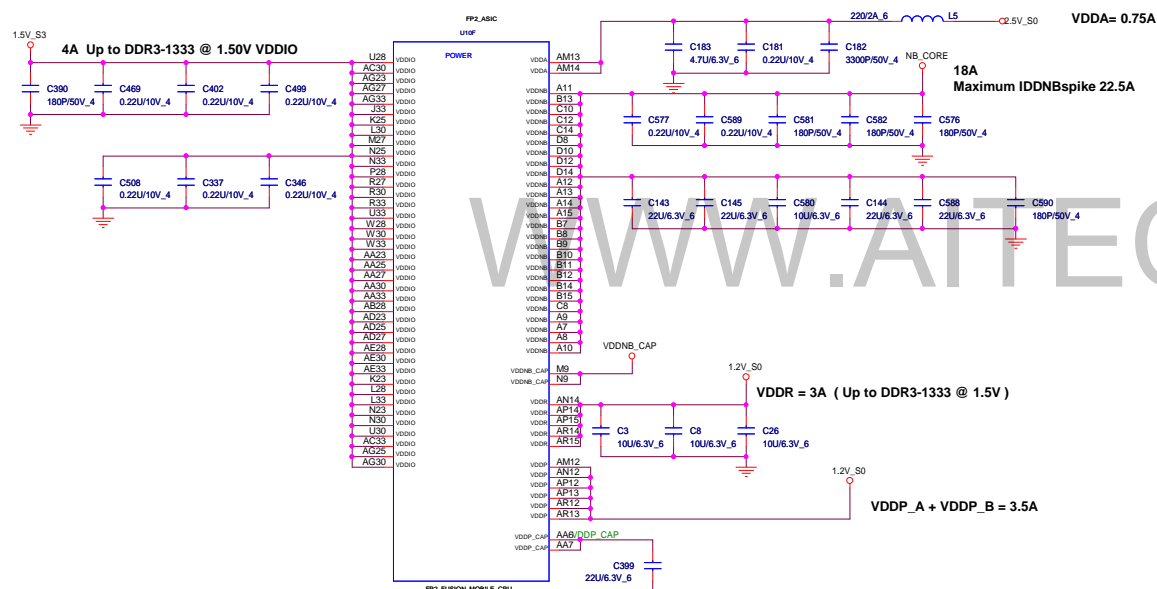
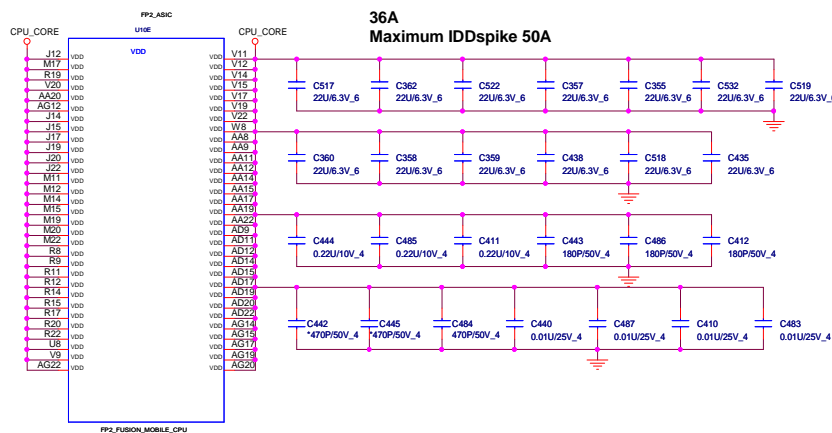




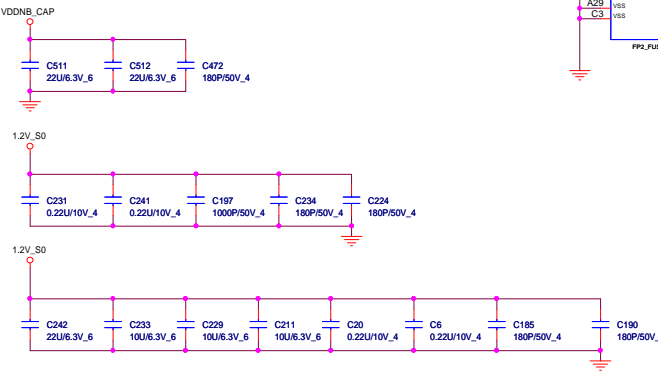
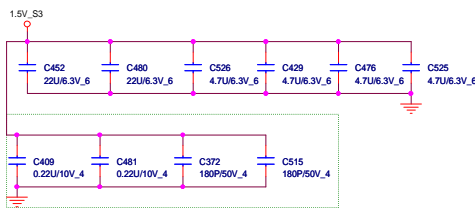
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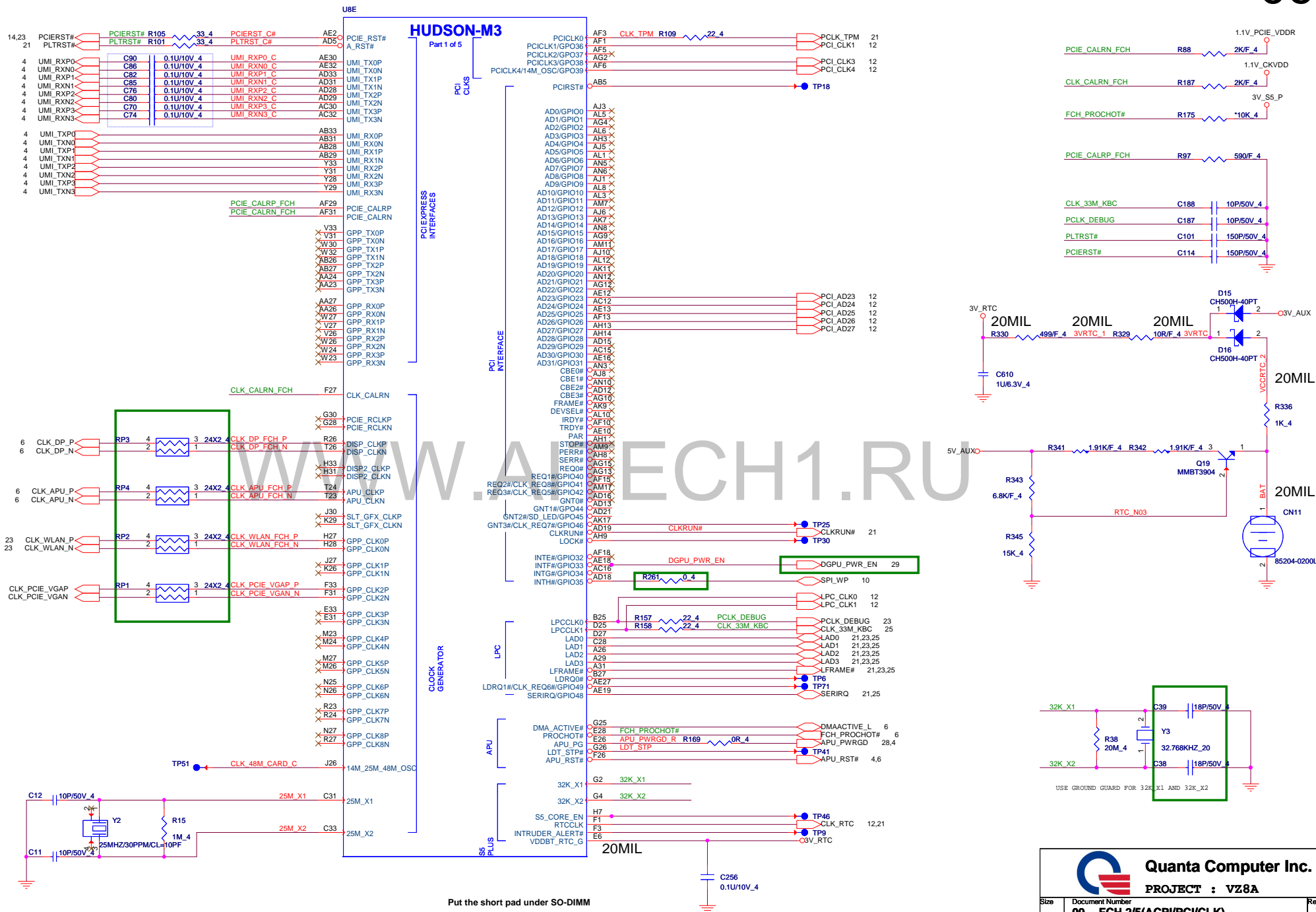


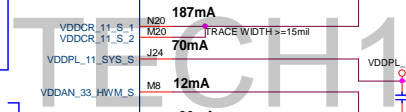
 Quanta Computer Inc. PROJECT : VZ8A		Rev 1A
Size	Document Number 06 -- APU 3/4(Display/Misc)	
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If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

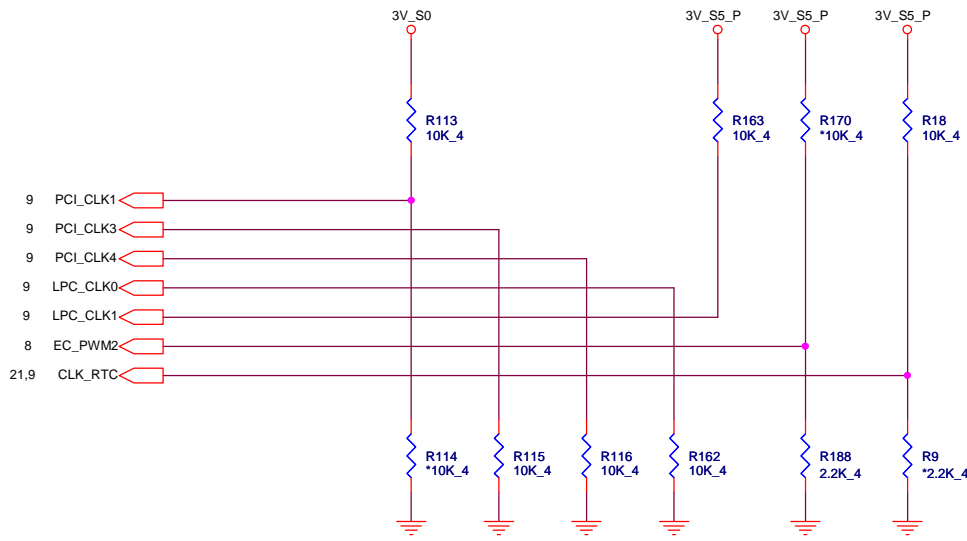






STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

Strap Pin	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
HIGH	ALLOW PCIE Gen2	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED	LPC ROM	S5 PLUS MODE DISABLED
LOW	FORCE PCIE Gen1	IGNORE DEBUG STRAP	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE

DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



Strap Pin	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

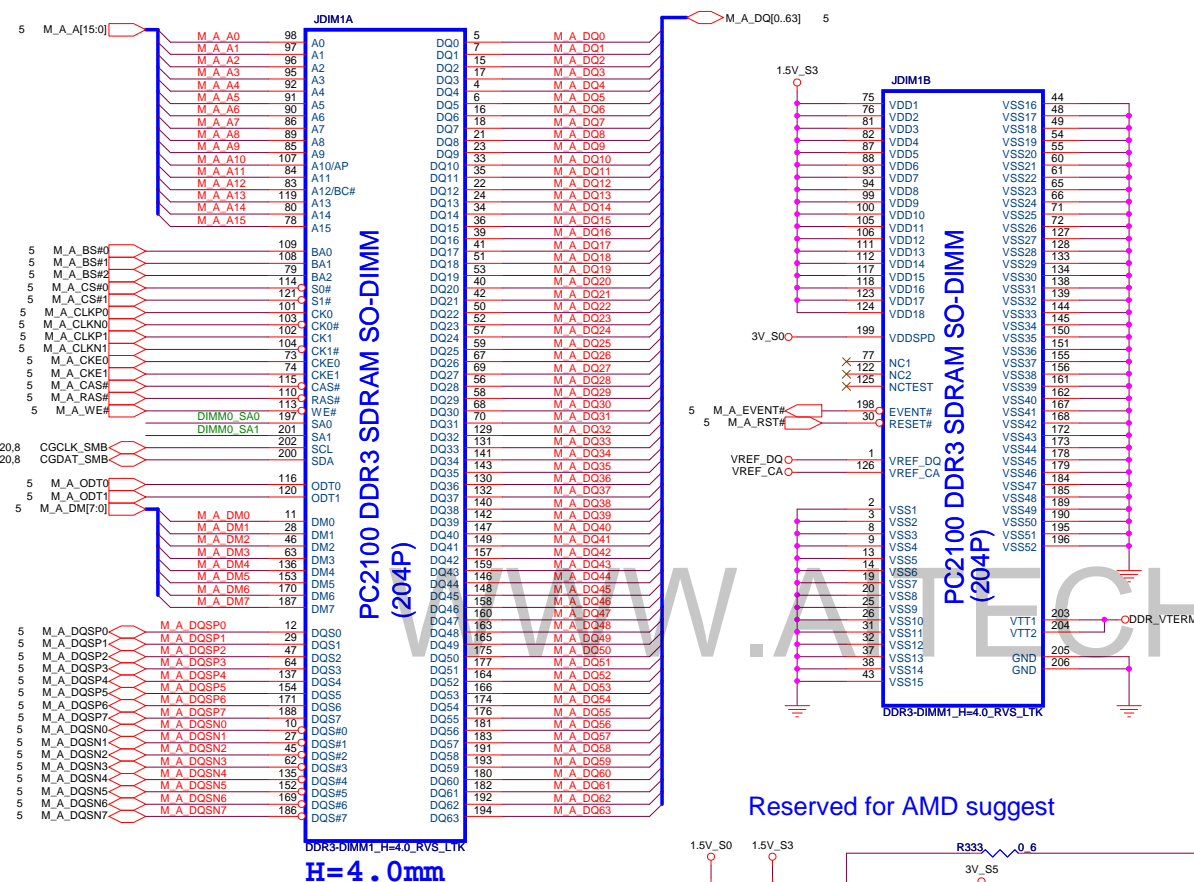
Quanta Computer Inc.
PROJECT : VZ8A

Size Document Number
12 -- FCH 5/5(Strap)

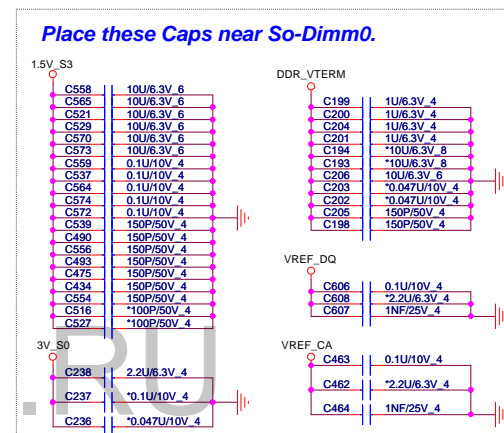
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Rev 1A

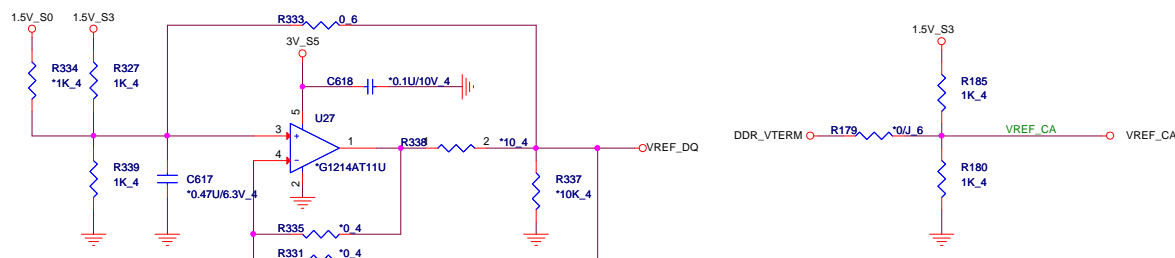
DDR_RVS(DDR)(CHA)

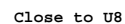


SMB ADD = A0



Reserved for AMD suggest





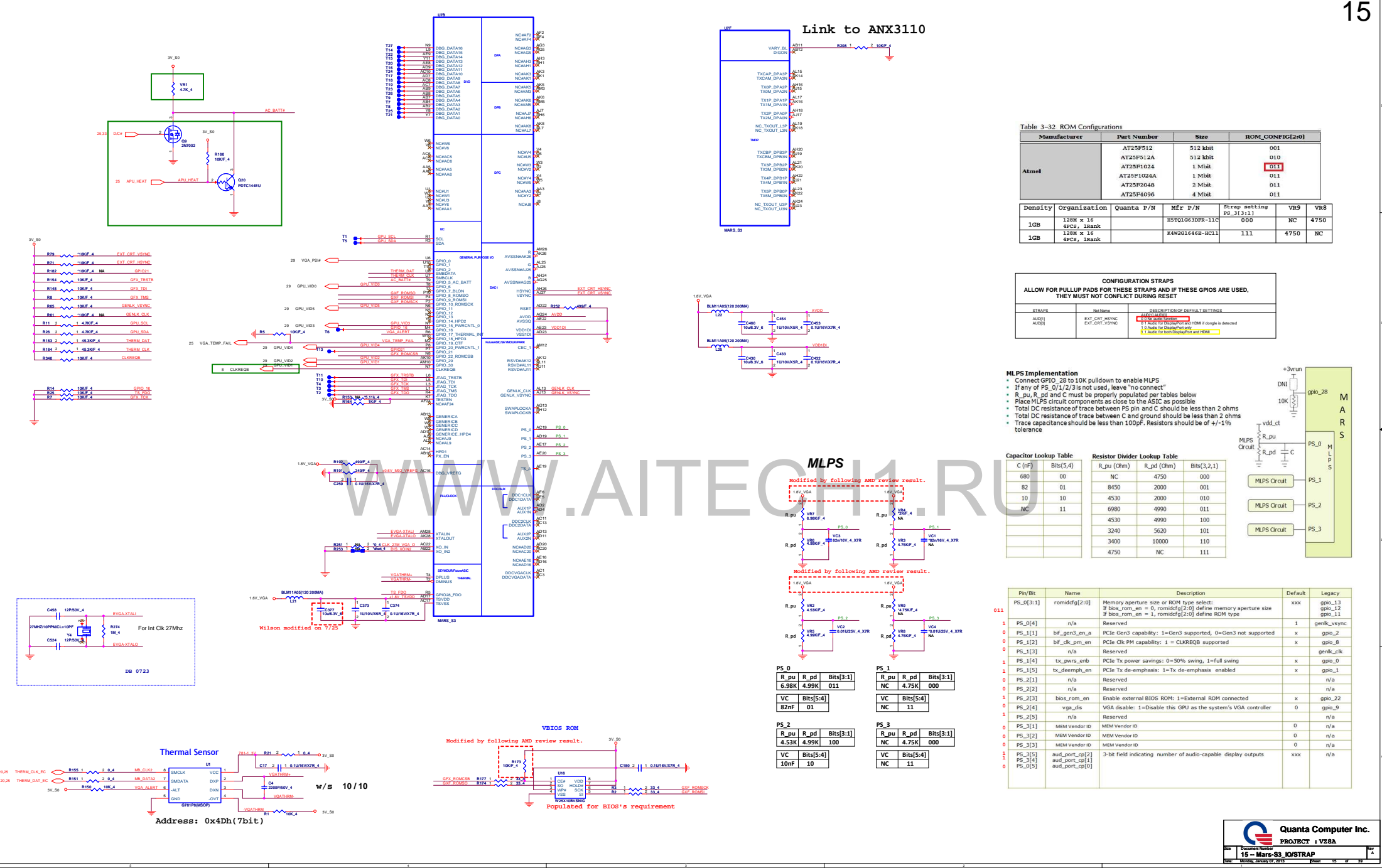


Table 3-32 ROM Configurations						
Manufacturer		Part Number	Size	ROM_CONFIG[2:0]		
Atmel		AT25F512	512 kbit		001	
		AT25F12A	512 kbit		010	
		AT25F1024	1 Mbit		011	
		AT25F1024A	1 Mbit		011	
		AT25F3048	2 Mbit		011	
		AT25F4096	4 Mbit		011	
Density	Organisation	Quanta P/N	Mfr P/N	Strap setting PS_3[3:1]	VR9	VR8
1GB	128K x 16 4PCS, 16bank		H5TQ1G630PR-11C	000	NC	4750
1GB	128K x 16 4PCS, 16bank		K4W2G1646E-RC11	111	4750	NC

CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PinName	DESCRIPTION/VALUE OF DEFAULT SETTINGS
AB10 AB05	EXT_CRT_VSYNC EXT_CRT_VSYNC	0: Audio for DisplayPort and HDMI 1 sample is detected 1: Audio for DisplayPort only 1.1: Audio for both DisplayPort and HDMI

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0[1:2] is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

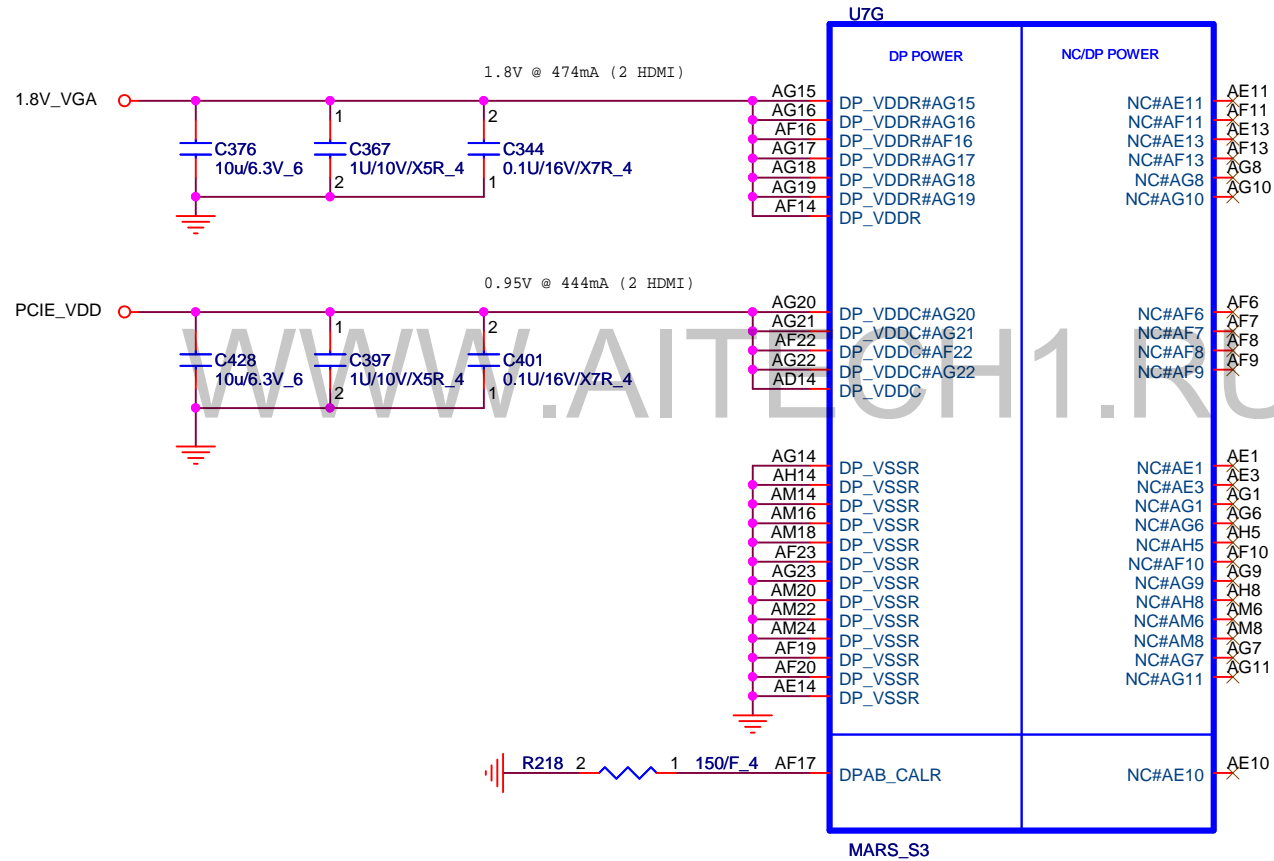
C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

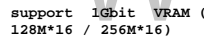
Resistor Divider Lookup Table

R _{pu} (Ohm)	R _{pd} (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

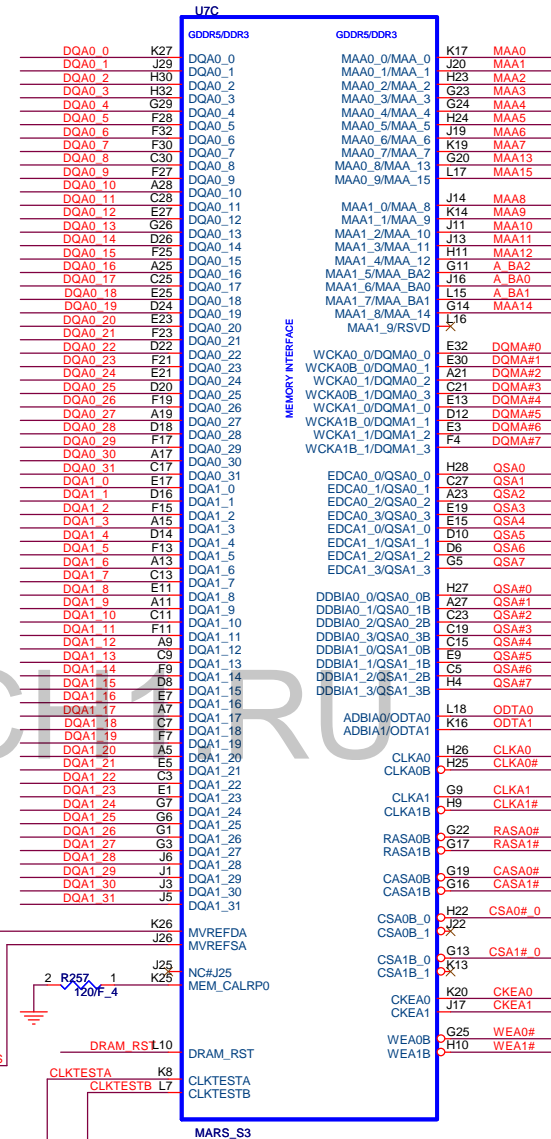
MLPS Circuit diagrams for PS_0, PS_1, PS_2, PS_3.

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidg[2:0] define memory aperture size If bios_rom_en = 1, romidg[2:0] define ROM type	xxx	gpo_13 gpo_12 gpo_11
PS_0[4]	n/a	Reserved		1 genk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpo_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQ supported	x	gpo_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwr5_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpo_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpo_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpo_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpo_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_3[5]	aud_port_cp[0]			

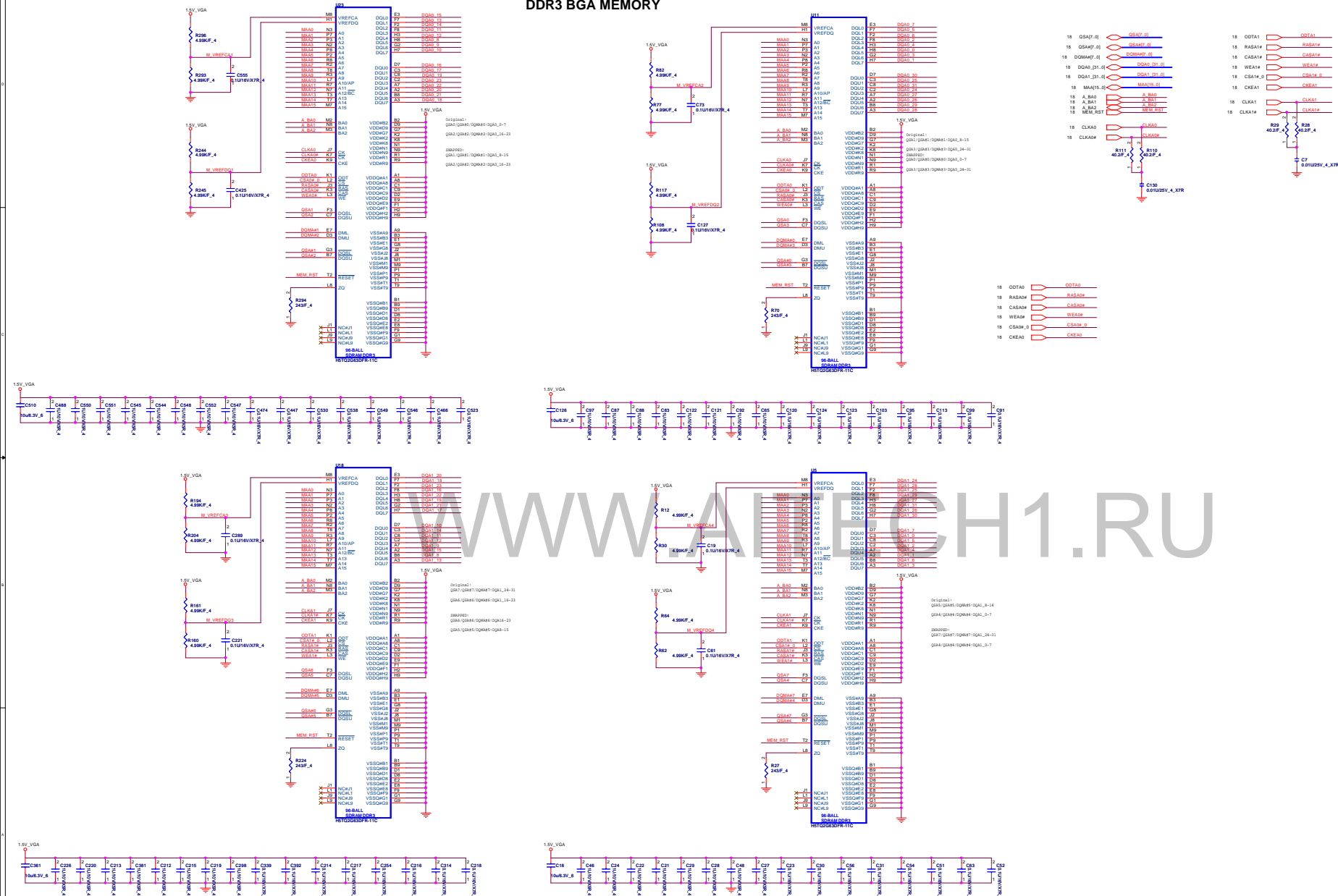


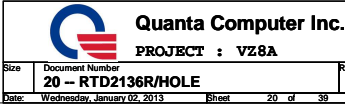


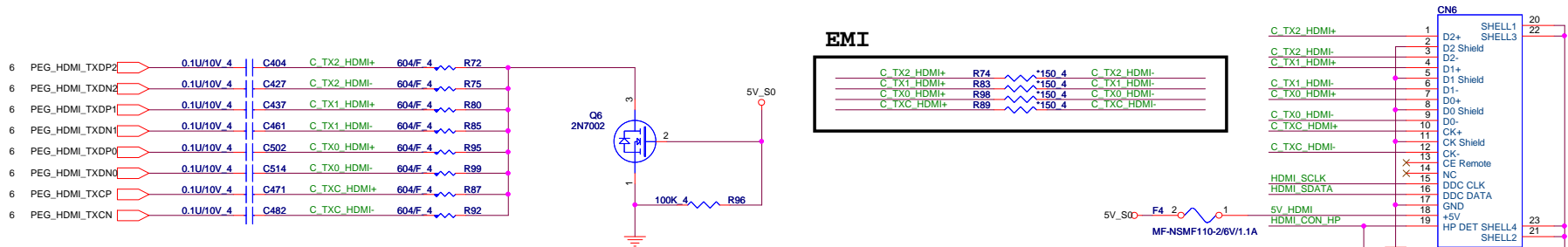
DRAM_RST PR132 1 2 10 4 R149 1 2 51.1/F 4 MEM_RST 19



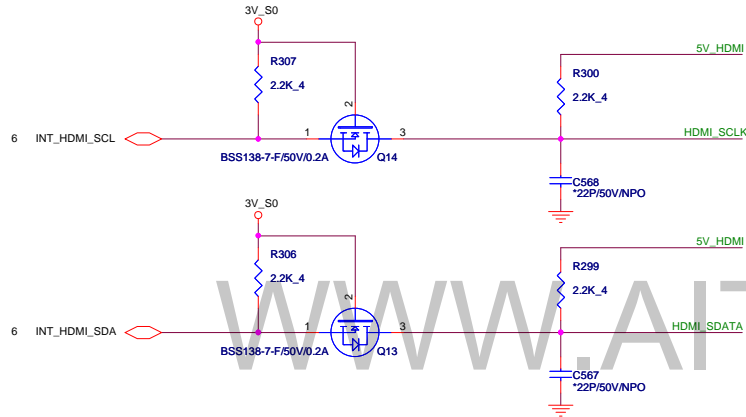
DDR3 BGA MEMORY







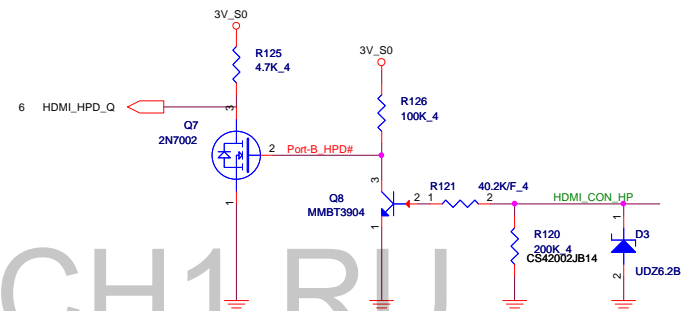
DDC Level Shift



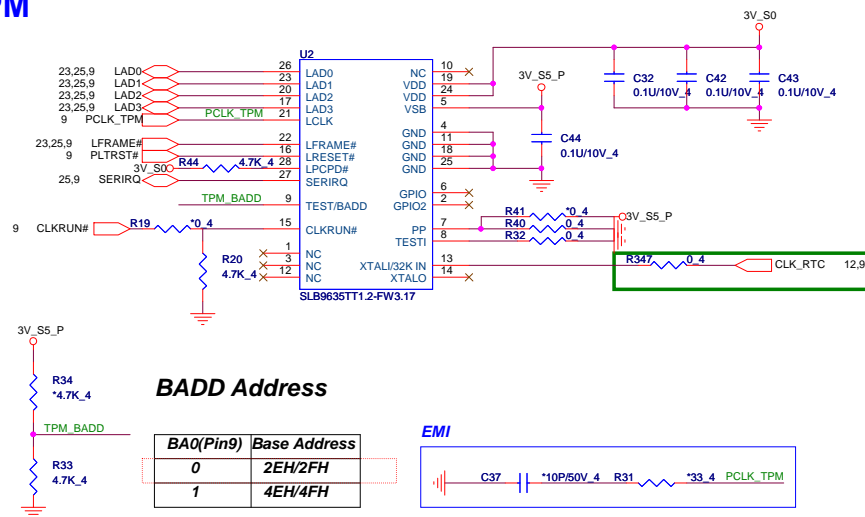
EMI

C_TX2_HDMI+	R74	*150_4	C_TX2_HDMI-
C_TX1_HDMI+	R83	*150_4	C_TX1_HDMI-
C_TX0_HDMI+	R98	*150_4	C_TX0_HDMI-
C_TXC_HDMI+	R89	*150_4	C_TXC_HDMI-

HPD



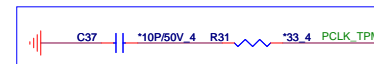
TPM



BADD Address

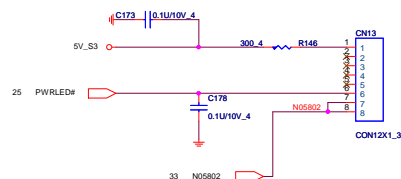
BA0(Pin9)	Base Address
0	2EH/2FH
1	4EH/4FH

EMI

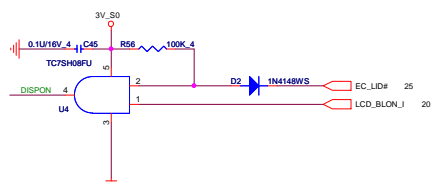


LED

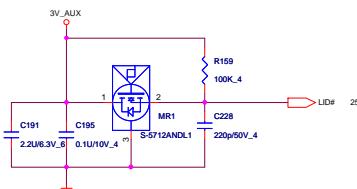
0.2A(20mils)



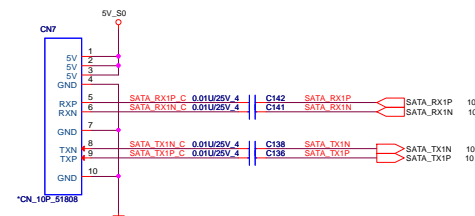
PANEL BACKLIGHT CONTROL



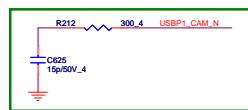
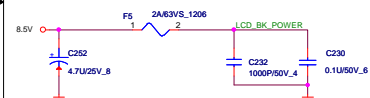
HALL
SENSOR&BACK
LIGHT SWITCH



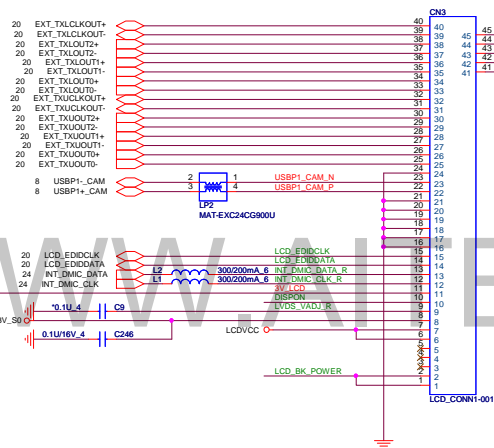
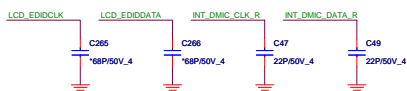
**SATA (SATA over FFC)
(Option)**



LCD Panel Module

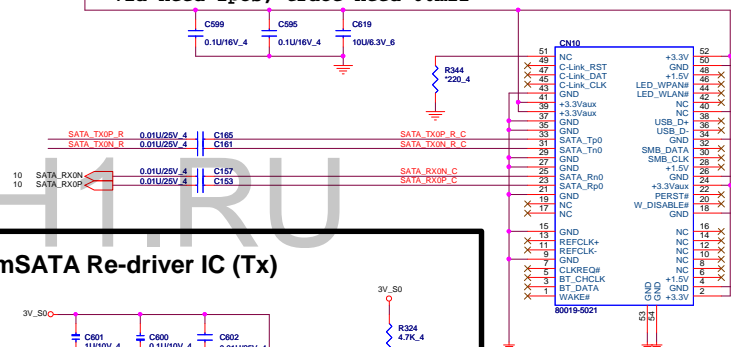


For EMI close to connector

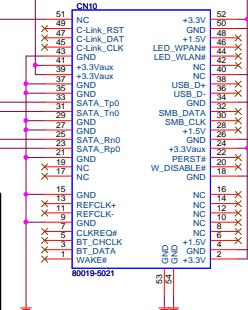
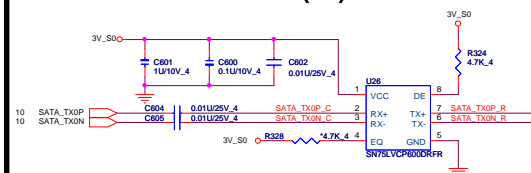


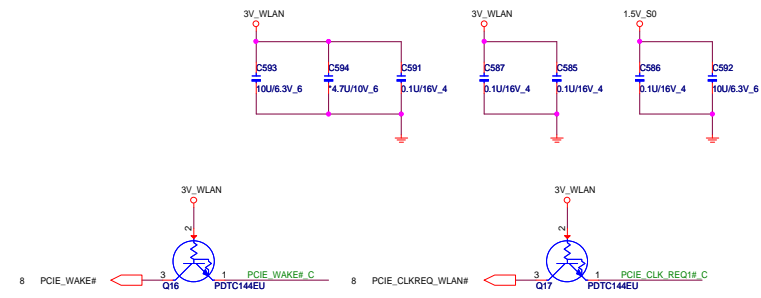
mSATA (SATA over mini PCIe)

128GB Write peak 4W, current 1.33A
Via need 2pcs, trace need 60mil

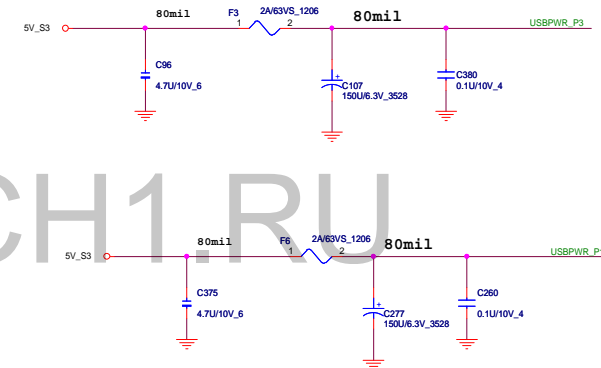


mSATA Re-driver IC (Tx)





Right Side for 15.6 only

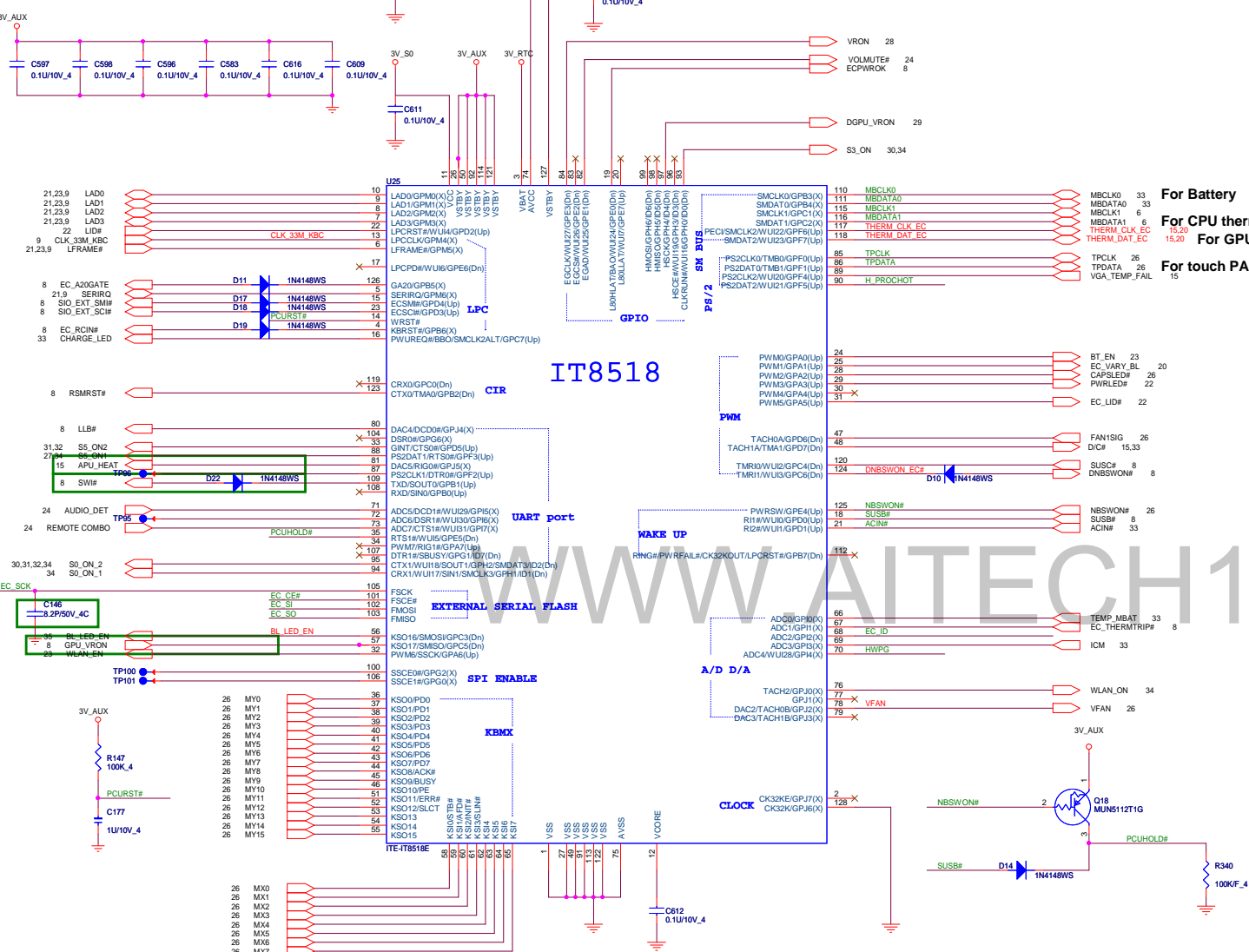


Typical Output Deemphasis

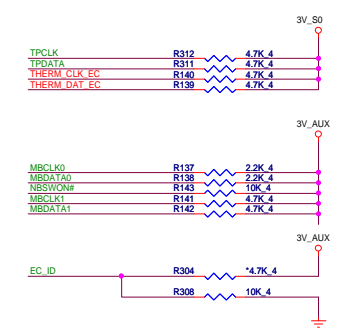
	OS = NC	OS = 0	OS = 1
DE = NC	3.8dB	2.9dB	4.3dB
0	6.0dB	5.1dB	6.4dB
1	7.9dB	7.0dB	8.3dB

EC_ITE8518G/HX

* Recommended net "3VPCU" and "VDDRTC" minimum trace width 12mils.

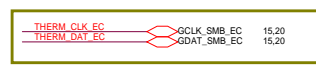


Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

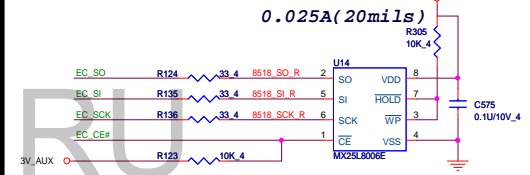


For Battery
For CPU thermal
For GPU thermal sensor
For touch PAD

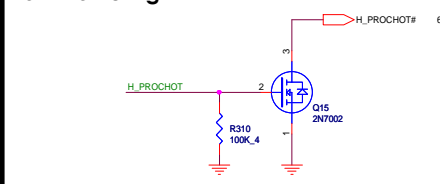
VZ7A	R113	Hi
VZ8A	R114	Lo



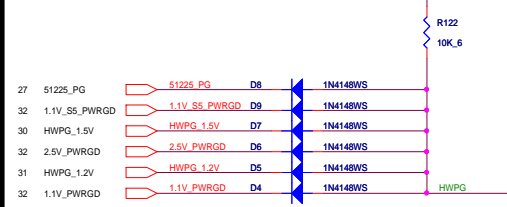
EC ROM 1MB



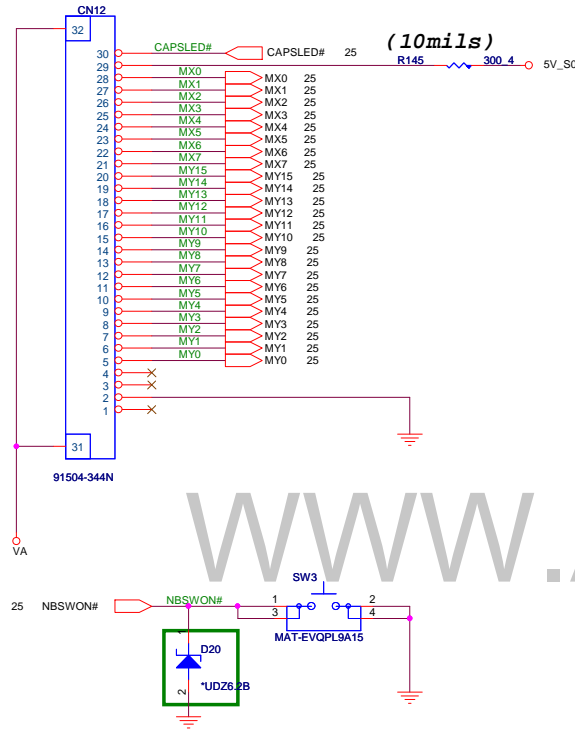
For throttling



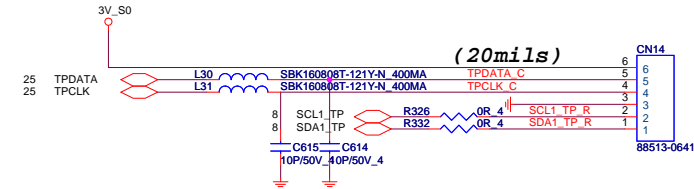
HWPG circuit



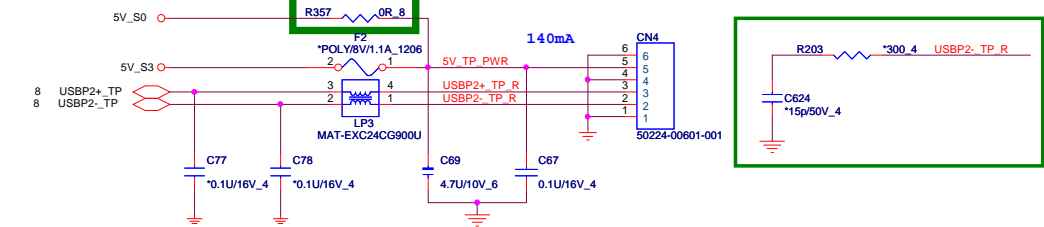
INT KeyBoard



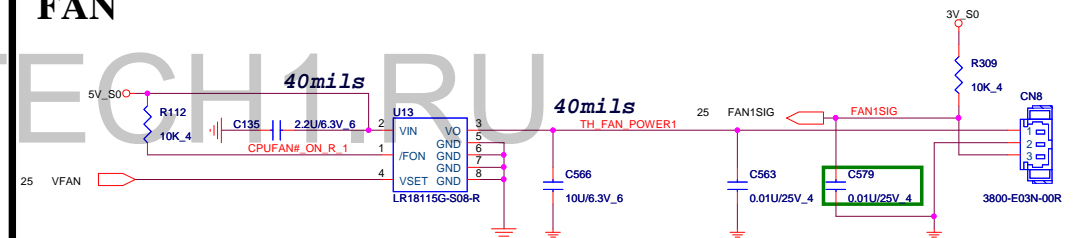
TP board



Touch Module

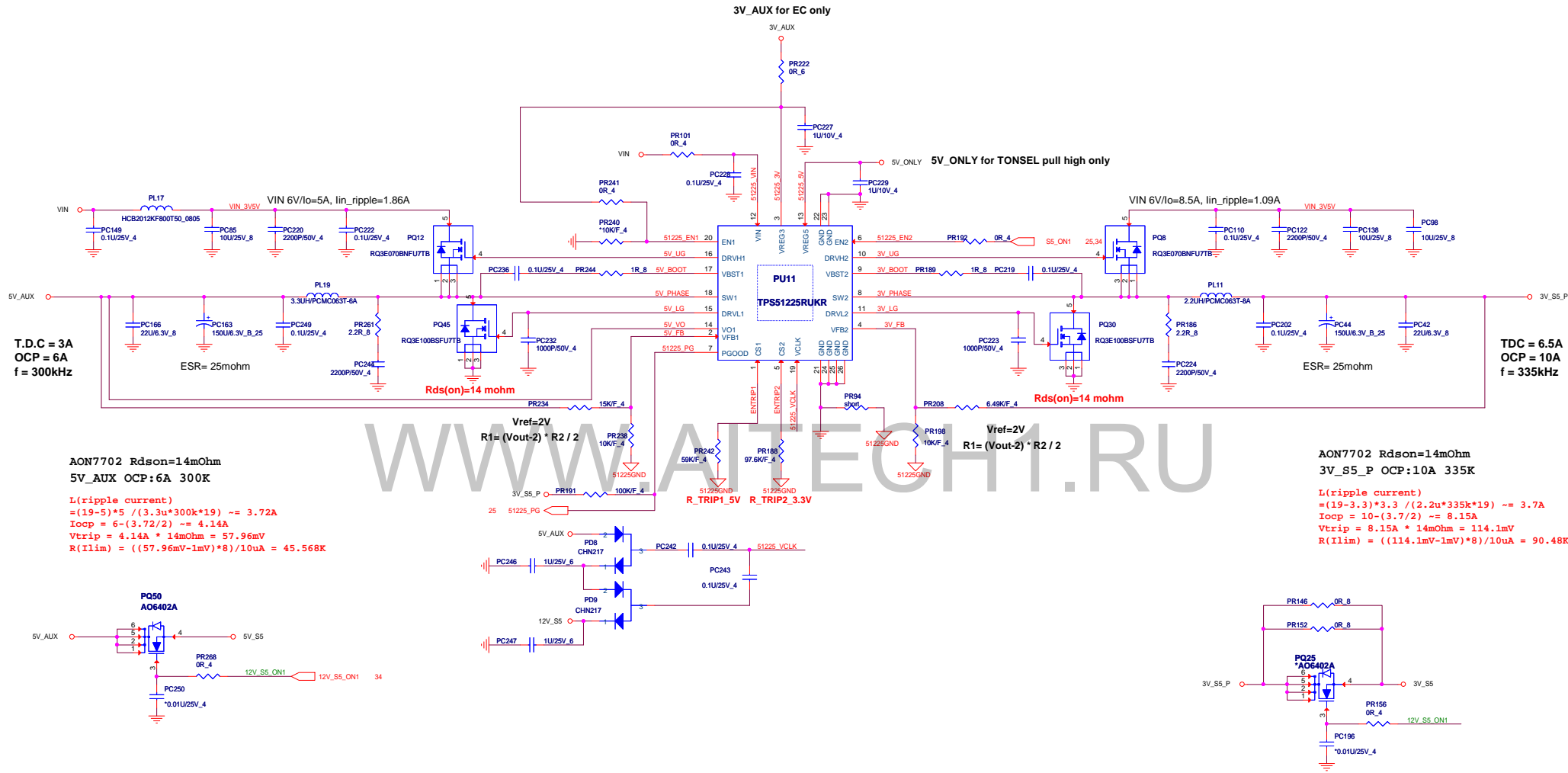


FAN



Quanta Computer Inc.
PROJECT : VZ8A

Size Document Number
26 -- TP/KB/FAN/Touch Module Rev
Date: Wednesday, January 02, 2013 Sheet 26 of 39 1A



AON7702 R_{ds(on)}=14mOhm
5V_AUX OCP:6A 300K
L(ripple current)
=(19-5)*5 / (3.3u*300k*19) ~ 3.72A
I_{ocp} = 6-(3.72/2) ~ 4.14A
V_{trip} = 4.14A * 14mOhm = 57.96mV
R(Ilim) = ((57.96mV-1mV)*8)/10uA = 45.568K

AON7702 R_{ds(on)}=14mOhm
3V_S5_P OCP:10A 335K
L(ripple current)
=(19-3.3)*3.3 / (2.2u*335k*19) ~ 3.7A
I_{ocp} = 10-(3.7/2) ~ 8.15A
V_{trip} = 8.15A * 14mOhm = 114.1mV
R(Ilim) = ((114.1mV-1mV)*8)/10uA = 90.48K

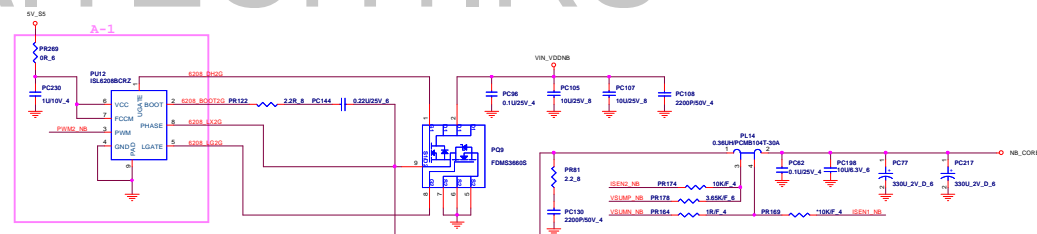
$$I_{ripple} = (V_{in} - V_{out}) * V_{out} / (V_{in} * L * f)$$

O.C.P setup information

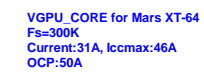
Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V	14m_Max	6	3.72	300	3.3uH	45.3K
3.3V	14m_Max	10	3.7	335	2.2uH	90.9K


Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

[illegible]

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	CYN	CV+36V0MZ13	30	50	1.2m Max.	11X10X4	PCMB104T-R36MT



 Quanta Computer Inc. PROJECT : VZ8A		
Size	Document Number 29--VGA_CORE(NCP3218MNR2G)	Rev 1A
Date:	Wednesday, January 10, 2018	Sheet 29 of 30



AON7702 Rdson=14mOhm
1.5V_S3 OCP:15A 400K

```
L(ripple current)
=(19-1.5)*1.5 /(1u*400k*19) ~= 3.45A
Iocp = 15-(3.45/2) ~= 13.275A
Vtrip = 13.275A * 14mOhm = 185.85mV
R(Ilim) = ((185.85mV*8)/10uA) = 148.68k
```

$$I_{ripple} = (V_{in} - V_{out}) * V_{out} / (V_{in} * L * f)$$

O.C.P. setup information

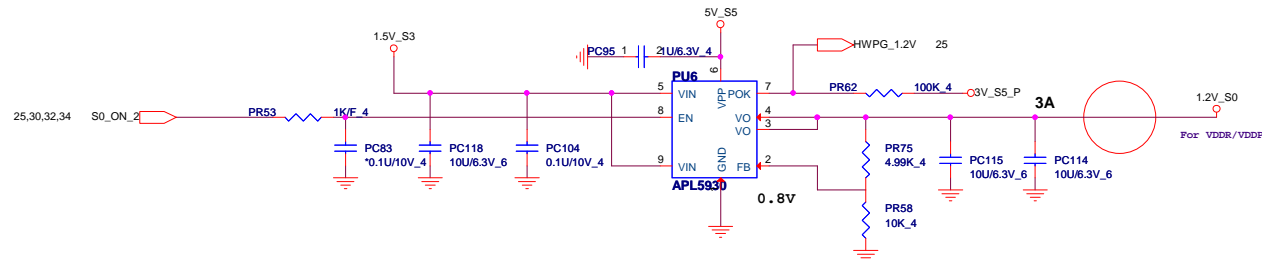
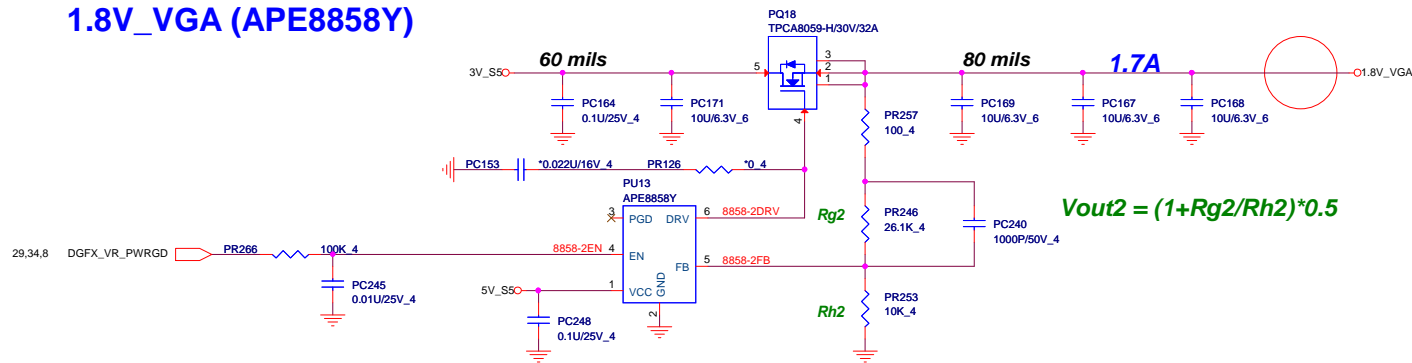
Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.5V	14m_Max	15	3.45	400	1uH	11.5K

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max
FDMC7692S	DFN 3*3	12.5A/18A	12m
AON7702	DFN 3*3	13.5A/20A	14m

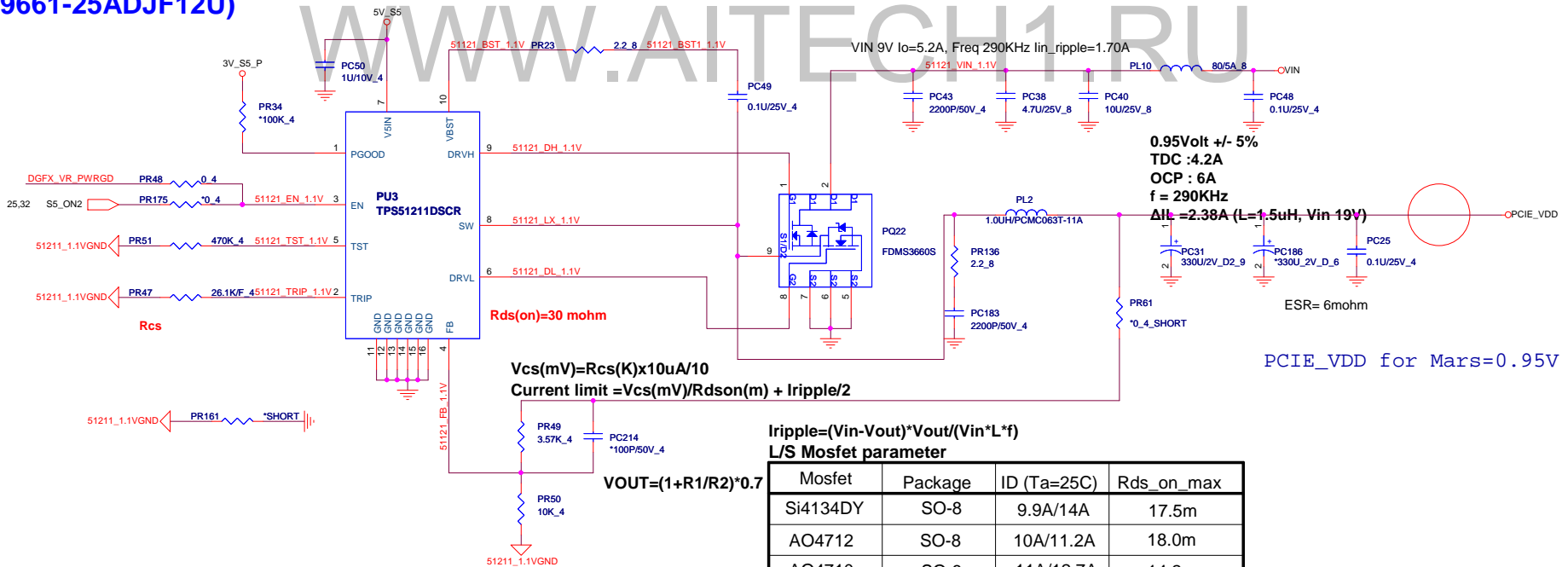
27,28,29,31,33,34	VIN	
27,28,31,32,34	5V_S5	
13,28,31,32,36,4,5,6,7	1.5V_S3	
13	DDR_VTERM	

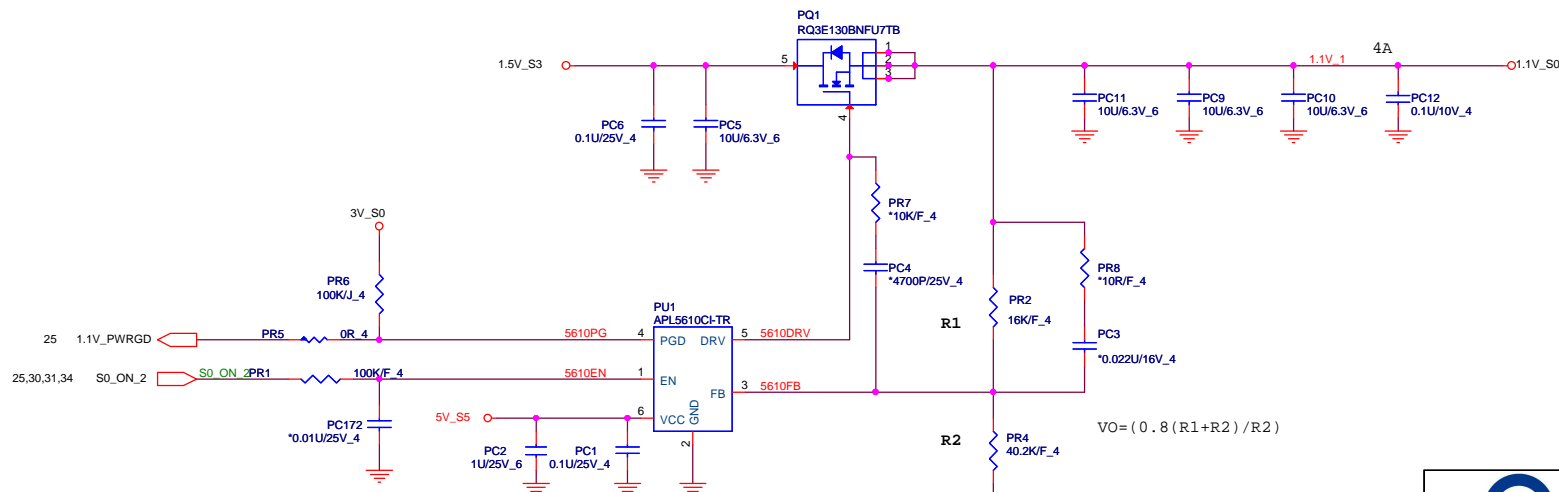
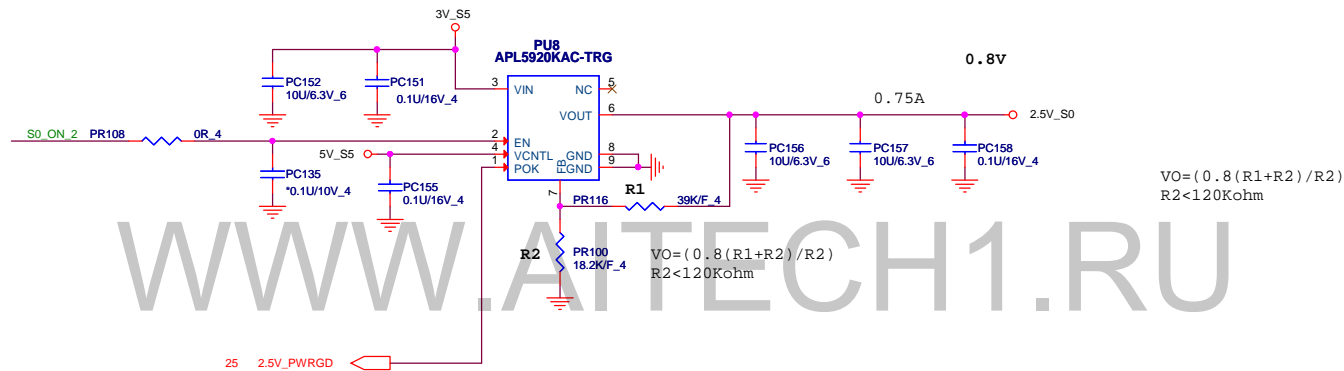
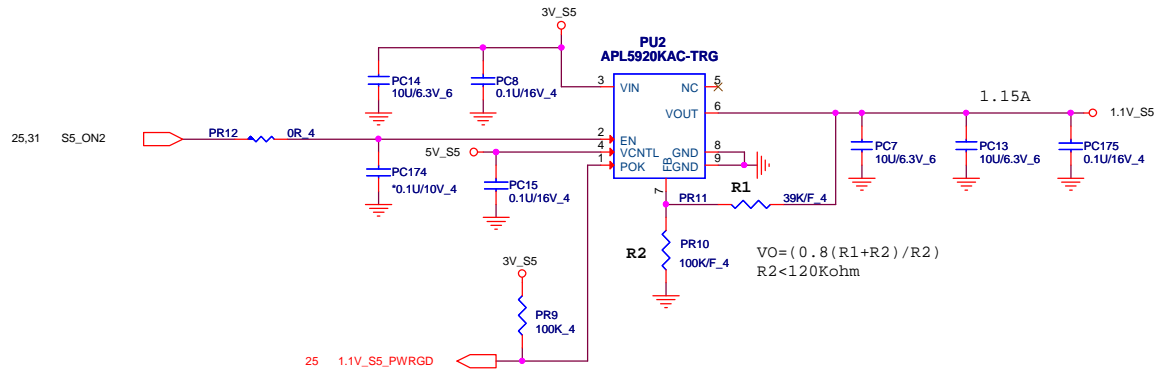
1.8V_VGA (APE8858Y)



$$V_{out} = 0.8(1 + R_1/R_2) = 1.2V$$

PCIE_VDD(G9661-25ADJF12U)





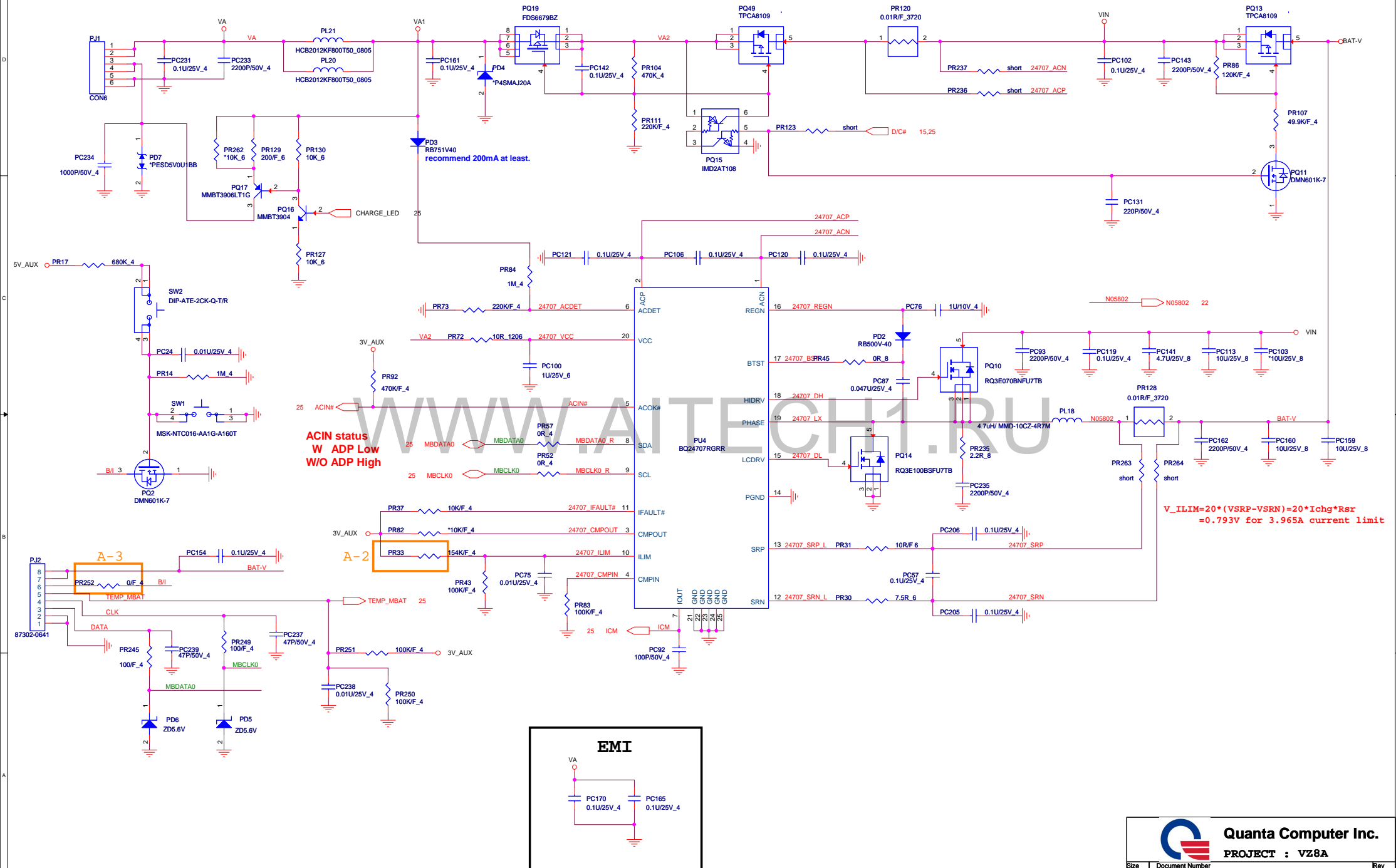
Quanta Computer Inc.

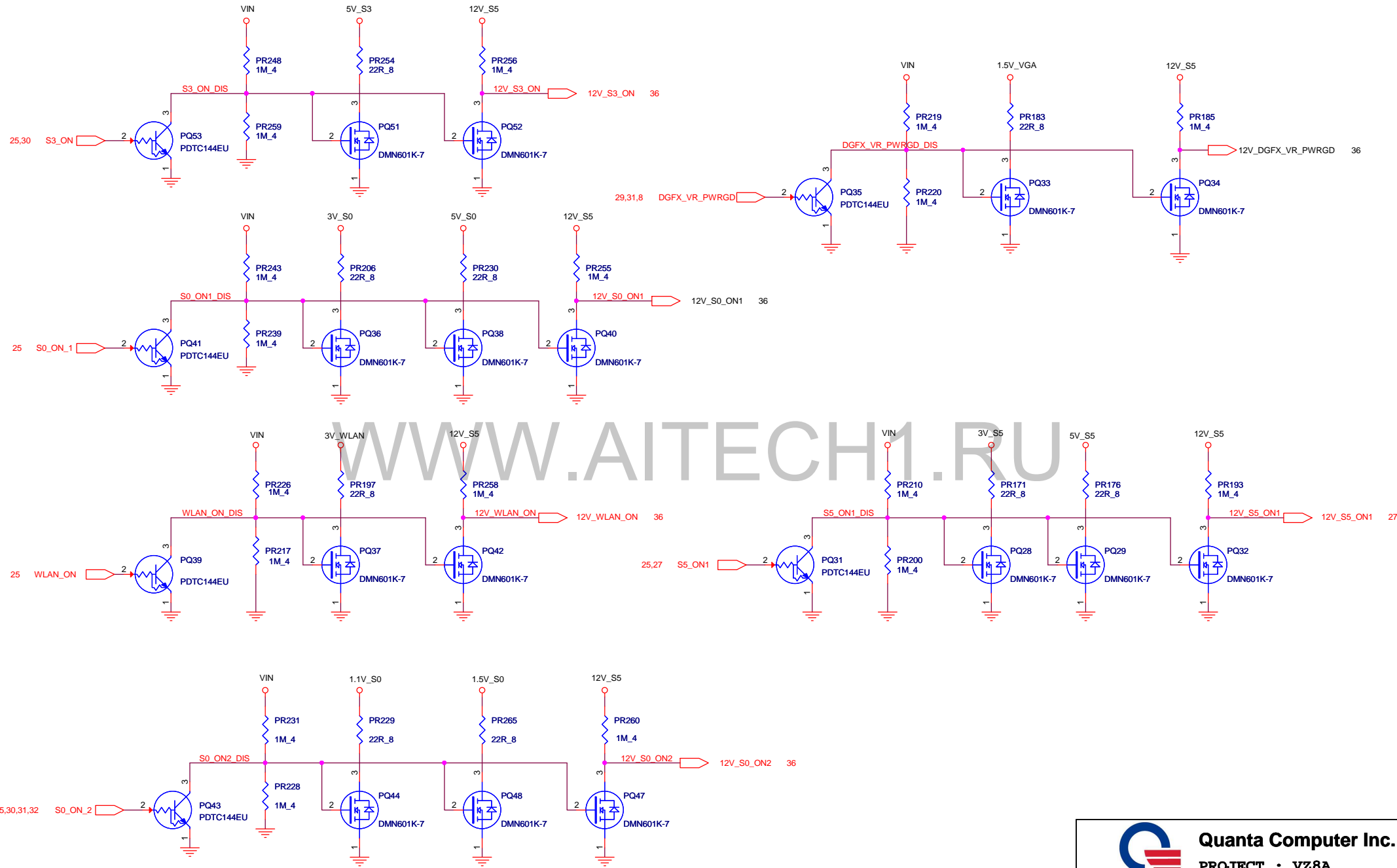
PROJECT : VZ8A

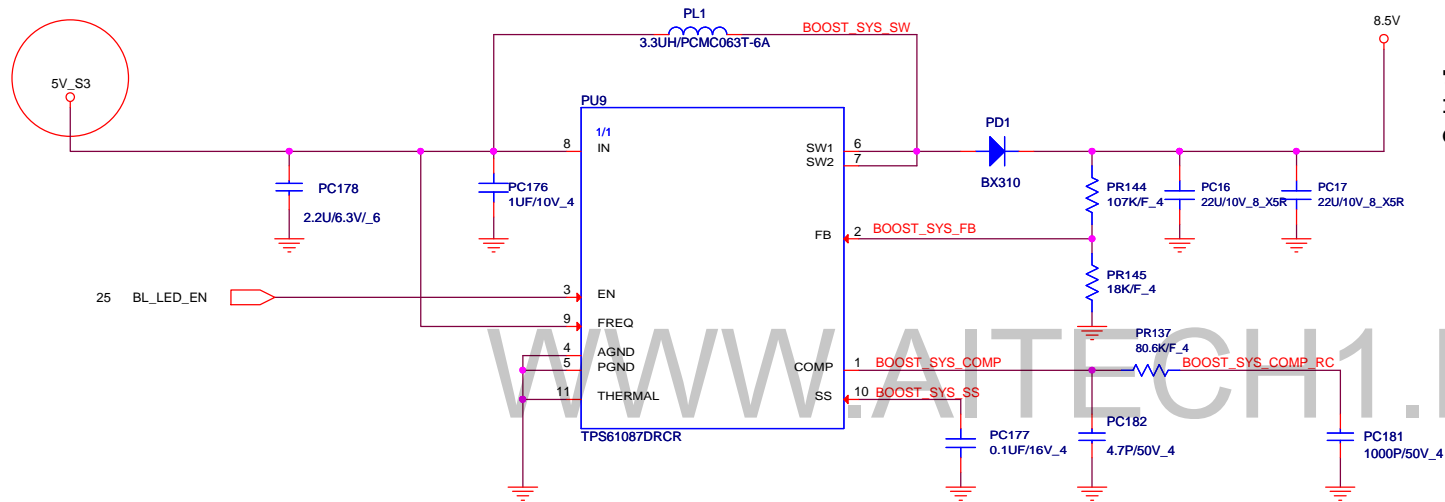
Size	Document Number	Rev
	32 - 1.1V_S5/2.5V/1.1V	1A
Date:	Wednesday, January 02, 2013	Sheet 32 of 39

Vga 10V, Id= 13A, Rdson 9m Max.,

Vga 10V, Id= 13A, Rdson 9m Max.,







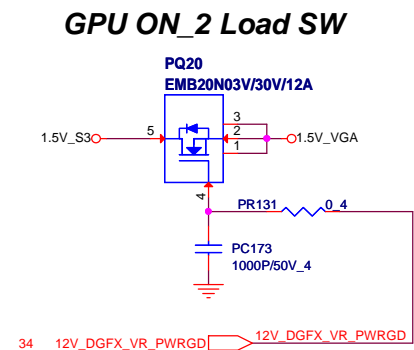
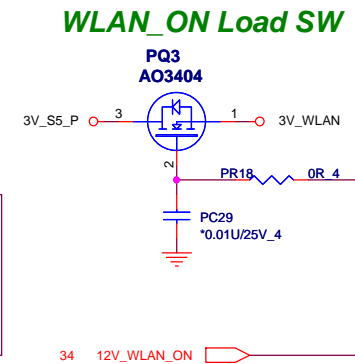
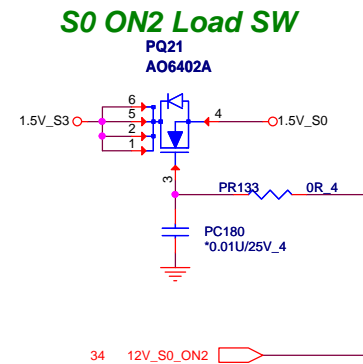
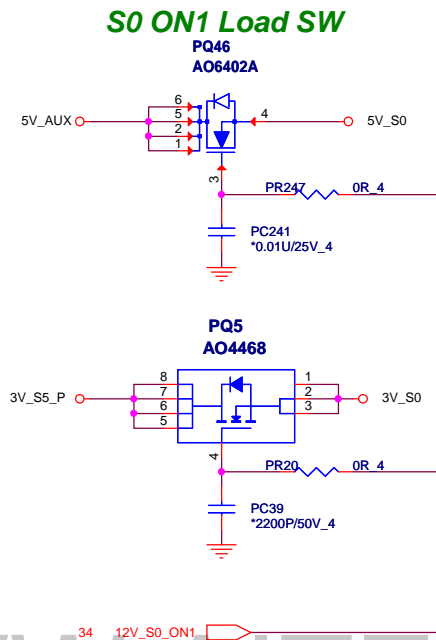
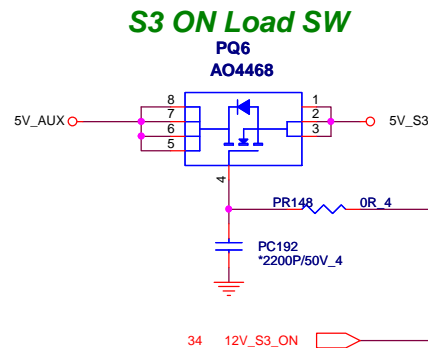
Quanta Computer Inc.

PROJECT : VZ3A

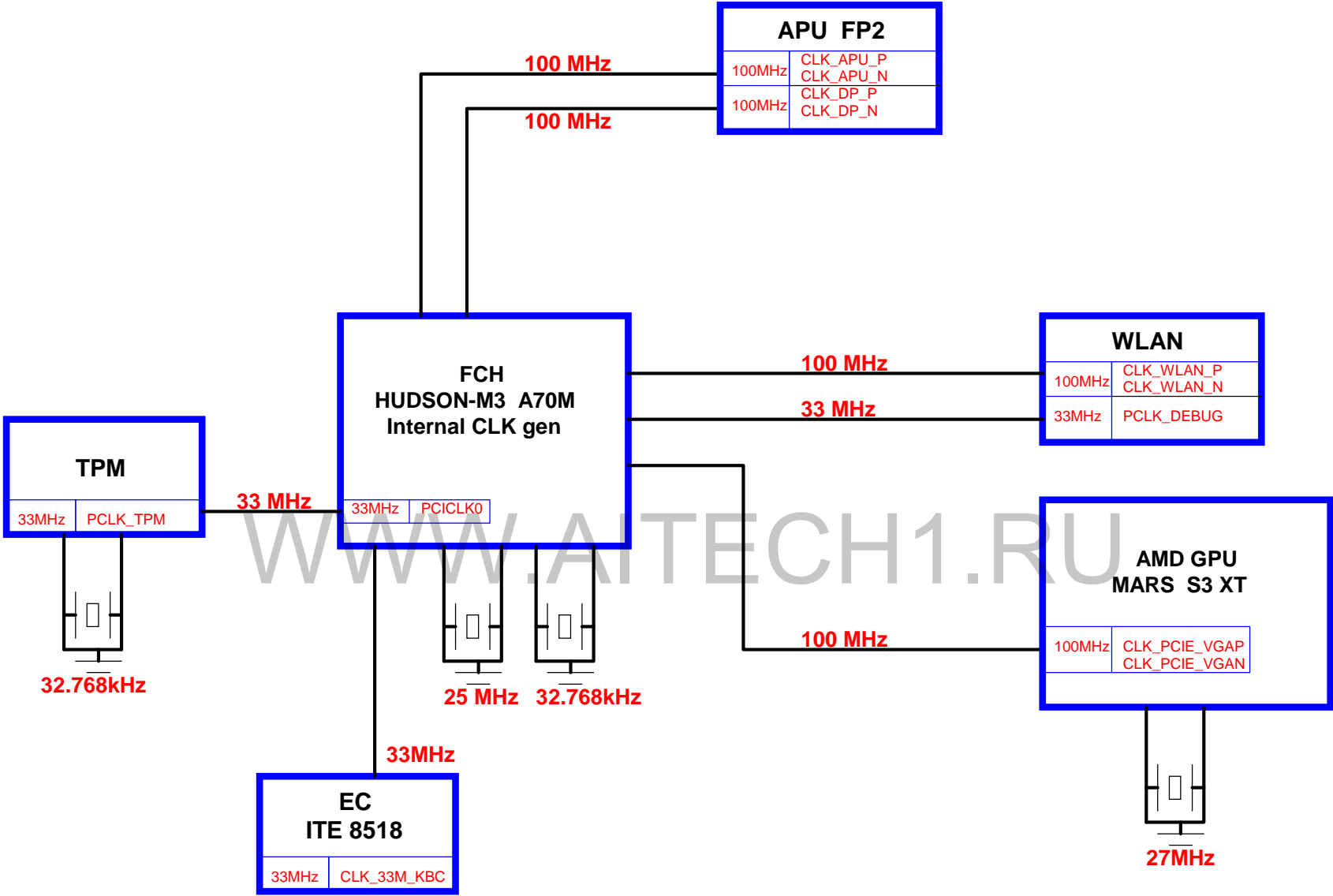
Size	Document Number	Rev
	35 -- 8.5V (TPS61087DRCR)	1A
Date:	Wednesday, January 02, 2013	Sheet 35 of 39

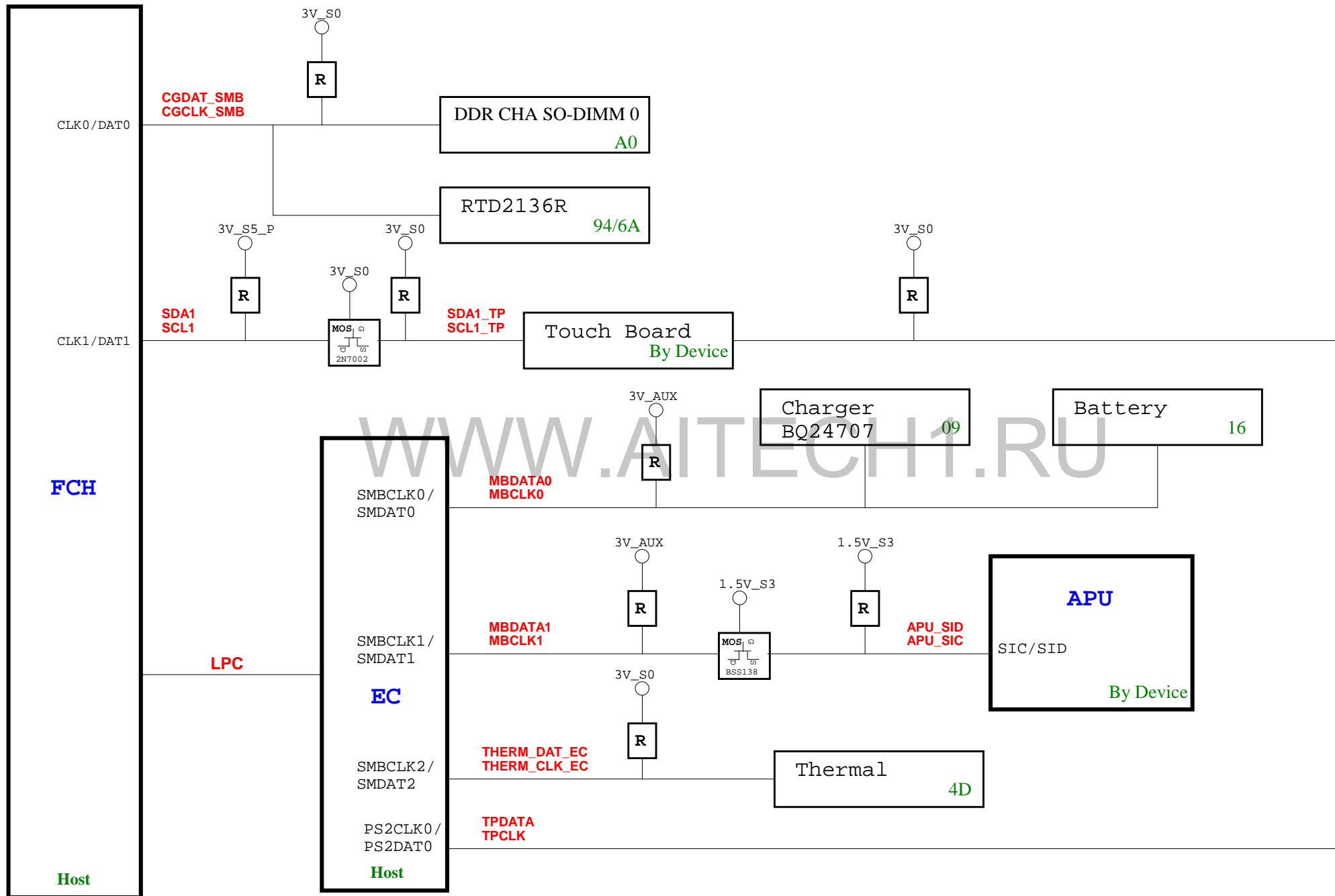
Load Switch

36




WWW.AITECH1.RU





39

Model	REV	CHANGE LIST														
VZ8A MB	A->B	<p>A-1: Add PR269, PU12 changes to ISLL6208BCRZ(AL006208005)</p> <p>A-2: Change PR33 to 154k ohm (CS41542FB16)</p> <p>A-3: Change PR252 to 0 ohm (CS00002JB38)</p> <p>A-4: Change U7 to AJ084200T13</p> <p>A-5: Insert R200, R201, R235 for USB3 driving control</p> <p>A-6: Change CN14 to DFFC06FR024 for SMT request</p> <p>A-7: Remove R118 , dd R119 and Del U12, C105 DP_PWM connect to scalar directly</p> <p>A-8: Del VR2 Change VR5 to 4.75k CS24752FB12 (Keep use external VBIOS ROM)</p> <p>A-9: C38,C39 from 12p change to 22p</p> <p>A-10: Del Y1, C1, C2 and add R347 TPM clock change to FCH</p> <p>A-11: Del R166, R167 (VID change to power portion)</p> <p>A-12: Add C621, C622 0.1uF for WLAN</p> <p>A-13: Remove R144 and add R325 VGA power EN change to EC</p> <p>A-14: Add U28, C620, R352 and R351 (layout reserve R351) for dGPU reset</p> <p>A-15: Add D22 for S3 LID from LID function</p> <p>A-16: GPU_VRON connector to EC, DGFY_VR_PWRGD</p> <p>A-17: Page31 DEL PR267(10Mohm) for 1.8V_VGA, DEL PR66(10Mohm) for 1.2V_S0, DEL PR134(10Mohm) for PCIE_VDD</p> <p>A-18: Pag.32 PU2/1.1V_S5 circuit modify from APL5920 to APL5930</p> <p>A-19: Pag.35 input voltage from 5V_AUX to 5V_S3, Page 28 reserve PR270</p> <p>A-20: add R321, R317 for WLAN pull high</p> <p>A-21: Reserve D20(NBSWON#), D21(ACZ_RST#_AUDIO) PN:BC512501Z00 for ESD requirement</p> <p>A-22: Y4 change to 3235 size, Add R261 for BIOS WP</p> <p>A-23: Add R357 for Touch Panel S0 power rail</p> <p>A-24: Add R358 for ESD</p> <p>A-25:Remove VGA debug circuit DEL CN1, C25, C128, C131, C132, C133, C134, C137, C139, C140 , C100, C98, C275, C282, R13, R22, R202, R212, R216, R198 , R203, R213, R217 CRT debug circuit</p> <p>A-26: Power change: Pag.32 (1.1V_S5) 回復APL5920 線路</p> <p>Pag.28 PR85 change from 866 OHM to 604 OHM(CS15042FB24) PC132 change from 0.022uf to 0.068uf(CH3683K9B00) PR55 change from 137K to 33K(CS33302FB14) PR91 change from 576 OHM to 562 ohm(CS15622FB16) PC140 change from 0.022uf to NA PR69 change from 3.48K to 3.4K(CS23402FB08)</p> <p>Pag.29 PC147 CHANGE FROM 120P to 150P(CS15622FB16) PR119 change from 33K to 39.2K(CS33922FB15) PC137 change from 22P to 12P(CH01206JB05) PR76 change from 0 ohm to 19.6K(CS31962FB18) PR46 change from NA to 6.04K(CS26042FB00)</p> <p>A-27: Change Y4 to BG627000035 (small size)</p> <p>A-28: GPU 27MHz x'tal: Change C458, C524 from 27P to 12P; Change R274 from 10M to 1M</p> <p>A-29: Del CN7 (BOM option)</p> <p>A-30: Change MR1 PN to AL008248000 to substitute EOD component</p> <p>A-31: Change PQ1 to RQ3E130BNFU7TB(BAM01300001) for power request</p> <p>A-32: NI R298 R324 for power on POST hang up issue</p> <p>A-33: Insert R317, R321 for WLAN enable issue</p> <p>A-34: Add R261 0 ohm for BIOS ROM WP function</p> <p>A-35: Change RP1 RP2 RP3 RP4 to 24 ohm (CJ024042N10) for sys CLK SI solution</p> <p>A-36: Change FCH U8 to MP PN (AJ075500T60), GPU U7 to MP PN (AJ084200T22)</p> <p>A-37: Add C146 8.2pF (CH-8206TB04)and insert C579 0.01uF for EMI</p>														
	B->C	<p>B-1: Add R298, R324 by re-driver vendor suggestion</p> <p>B-2: Change U20 to AL001464000 for better part</p> <p>B-3: NI R200, R201, R235, insert R237 2k ohm(CS22002FB19) by re-driver vendor suggestion</p> <p>B-4: Reserve R203 and C624 (NI) R212 and C625 (Insert) for internal USB2.0 device workaroud</p> <p>B-5: Add Q20 R166 and net APU_HEAT for GPU throttling function</p> <p>B-6: VR1 change to 4.7k ohm</p> <p>B-7: Change C38 C39 to 18pF for Xtal accuracy by vendor</p>														
		<table><tr><td>DOC NO.</td><td>PROJECT MODEL:</td><td>VZ8A</td><td>APPROVED BY:</td><td></td><td>DATE:</td><td>2012/7/7</td></tr><tr><td></td><td>PART NUMBER:</td><td></td><td>DRAWING BY:</td><td></td><td>REVISION:</td><td>1A</td></tr></table>	DOC NO.	PROJECT MODEL:	VZ8A	APPROVED BY:		DATE:	2012/7/7		PART NUMBER:		DRAWING BY:		REVISION:	1A
DOC NO.	PROJECT MODEL:	VZ8A	APPROVED BY:		DATE:	2012/7/7										
	PART NUMBER:		DRAWING BY:		REVISION:	1A										



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PROJECT : VZ8A

39 -- Change list

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Date: 2012/7/7
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